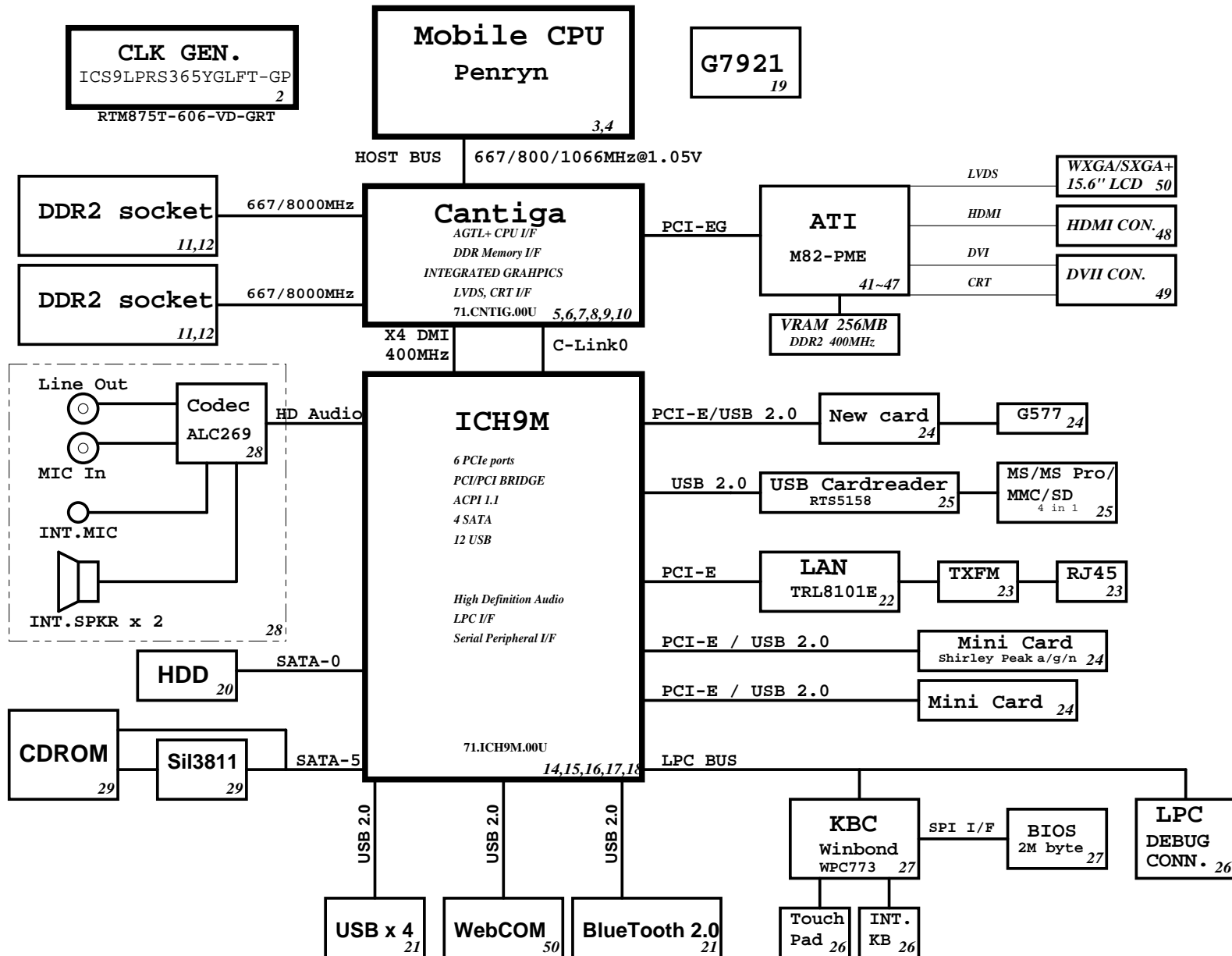


P08B1 Block Diagram

Project code: 91.4J701.001

PCB P/N : 08200

REVISION : -1



SYSTEM DC/DC TPS51125 32	
INPUTS	OUTPUTS
DCBATOUT	5V_S5(5A) 3D3V_S5(5A)

SYSTEM DC/DC TPS51124 34	
INPUTS	OUTPUTS
DCBATOUT	1D05V_M(11A) 1D8V_S3(10A)

RT9026 33	
1D8V_S3	DDR_VREF_S0(1.5A) DDR_VREF_S3

APL5912 33	
1D8V_S3	1D5V_S0

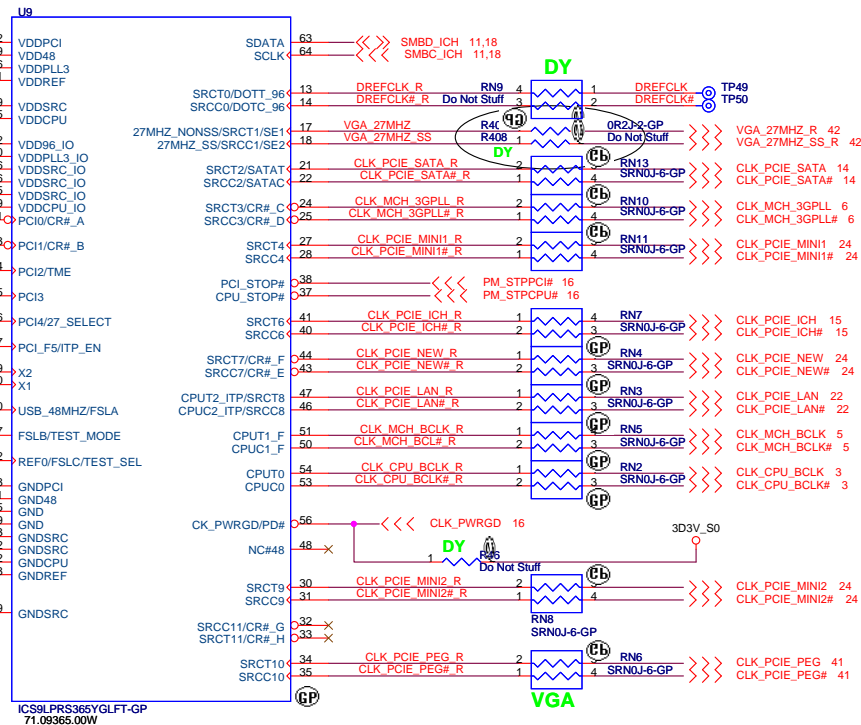
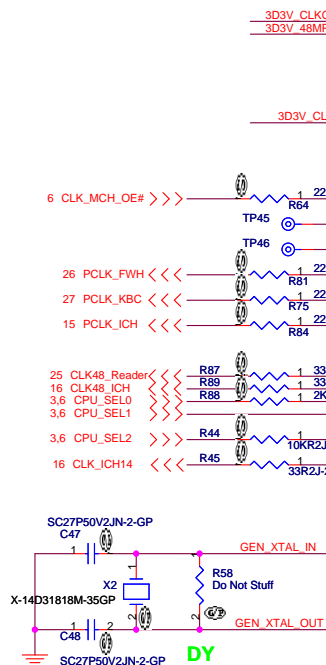
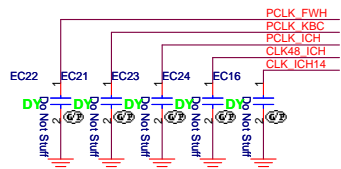
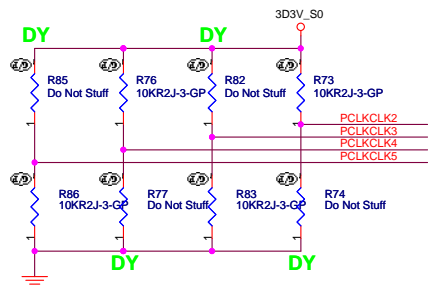
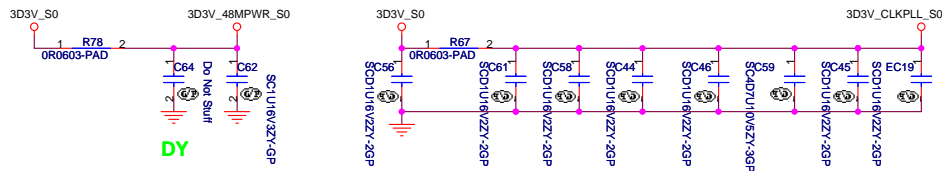
VGA DC/DC RT8202 40	
INPUTS	OUTPUTS
DCBATOUT	VGA_CORE

CHARGER MAX8731 37	
INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC ISL6266A 31	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 38A

BOM

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BLOCK DIAGRAM	
Size A3	Document Number
Date: Friday, May 23, 2008	Sheet 1 of 50
P08B1	
SA	



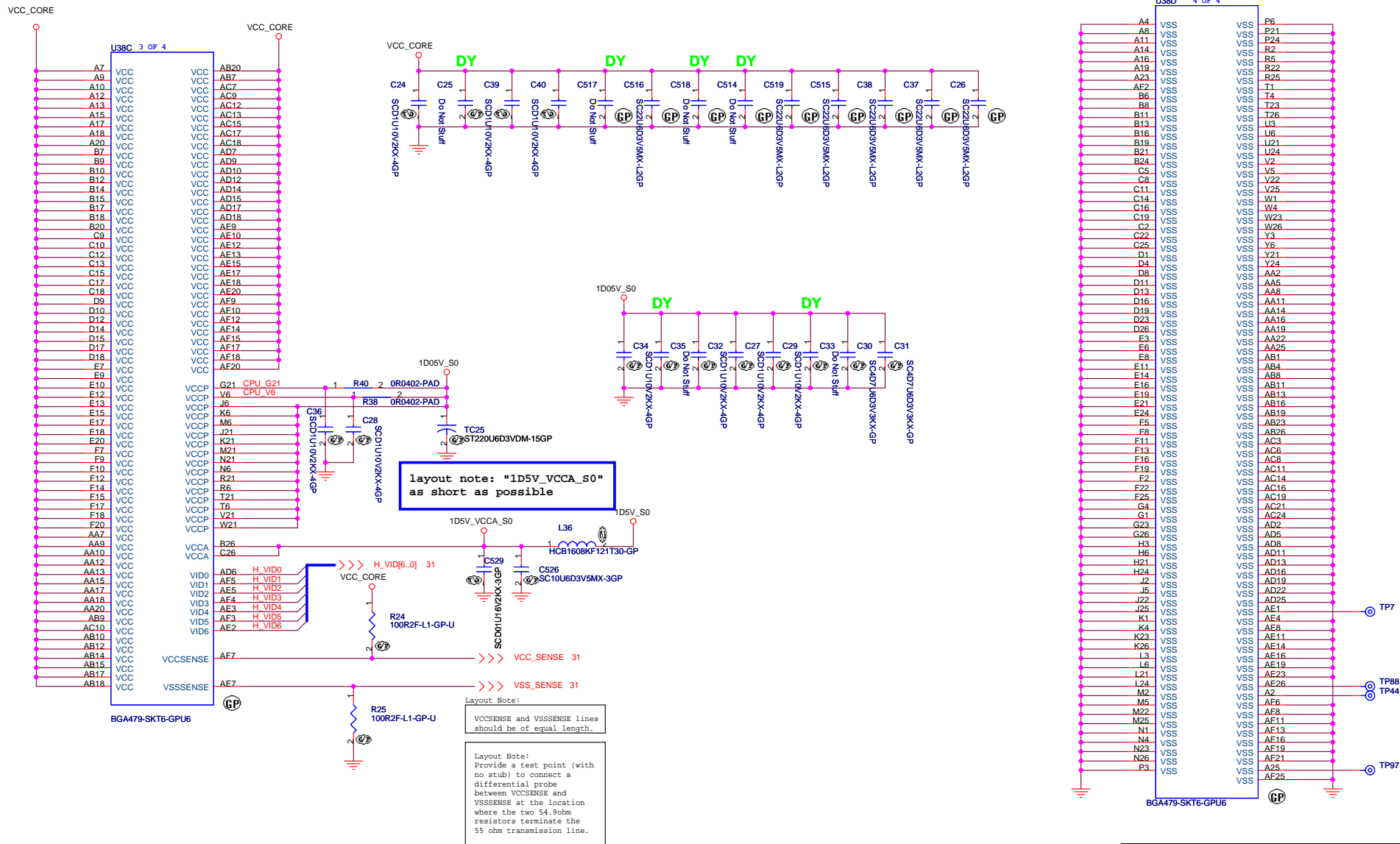
ICS9LPRS365YGLFT setting table

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3	0 = Pin37 as CPU_STOP# , pin 38 as PCI_STOP# 1 = Pins37,38 as SRC-3 differential pair.
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

SEL2	SEL1	SEL0	CPU	FSB
FSC	FSB	FSA		
1	0	1	100M	X
0	0	1	133M	533M
0	1	1	166M	667M
0	1	0	200M	800M
0	0	0	266M	1067M

BOM

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Clock Generator	
Title Size Date: Friday, May 23, 2008	Document Number P08B1 Sheet 2 of 50
Rev SA	

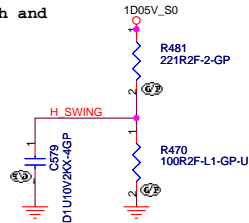


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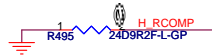
Title		
CPU (2 of 2)		
Size	Document Number	Rev
	P08B1	SA
Date: Friday, May 23, 2008		
Sheet	4	of 50

H_SWING routing Trace width and
Spacing use 10 / 20 mil

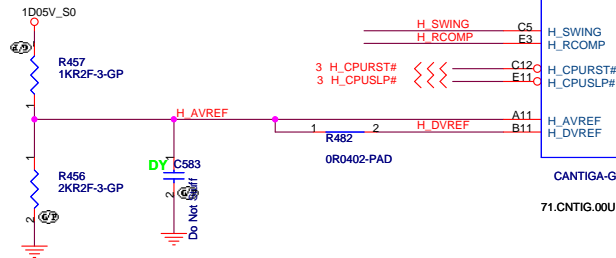
H_SWING Resistors and
Capacitors close MCH
500 mil (MAX)



H_RCOMP routing Trace width and
Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



U52A

1 OF 10

H_D#0 F2 H_D#_0
H_D#1 F8 H_D#_1
H_D#2 F8 H_D#_2
H_D#3 E6 H_D#_3
H_D#4 G2 H_D#_4
H_D#5 H6 H_D#_5
H_D#6 F2 H_D#_6
H_D#7 F2 H_D#_7
H_D#8 D4 H_D#_8
H_D#9 H3 H_D#_9
H_D#10 M9 H_D#_10
H_D#11 M11 H_D#_11
H_D#12 J2 H_D#_12
H_D#13 J2 H_D#_13
H_D#14 N12 H_D#_14
H_D#15 J6 H_D#_15
H_D#16 L2 H_D#_16
H_D#17 L2 H_D#_17
H_D#18 R2 H_D#_18
H_D#19 N9 H_D#_19
H_D#20 L6 H_D#_20
H_D#21 M4 H_D#_21
H_D#22 J3 H_D#_22
H_D#23 N2 H_D#_23
H_D#24 R1 H_D#_24
H_D#25 N5 H_D#_25
H_D#26 N6 H_D#_26
H_D#27 P13 H_D#_27
H_D#28 N8 H_D#_28
H_D#29 L7 H_D#_29
H_D#30 N10 H_D#_30
H_D#31 M3 H_D#_31
H_D#32 Y3 H_D#_32
H_D#33 AD14 H_D#_33
H_D#34 Y6 H_D#_34
H_D#35 Y10 H_D#_35
H_D#36 Y12 H_D#_36
H_D#37 Y14 H_D#_37
H_D#38 Y7 H_D#_38
H_D#39 W2 H_D#_39
H_D#40 A68 H_D#_40
H_D#41 Y9 H_D#_41
H_D#42 AA13 H_D#_42
H_D#43 AA9 H_D#_43
H_D#44 AA11 H_D#_44
H_D#45 AD11 H_D#_45
H_D#46 AD10 H_D#_46
H_D#47 AD13 H_D#_47
H_D#48 AE12 H_D#_48
H_D#49 AE9 H_D#_49
H_D#50 AA2 H_D#_50
H_D#51 AD8 H_D#_51
H_D#52 AA3 H_D#_52
H_D#53 AD3 H_D#_53
H_D#54 AD7 H_D#_54
H_D#55 AE14 H_D#_55
H_D#56 AE3 H_D#_56
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H_D#58 AE3 H_D#_58
H_D#59 AC3 H_D#_59
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H_D#62 AG2 H_D#_62
H_D#63 AD6 H_D#_63

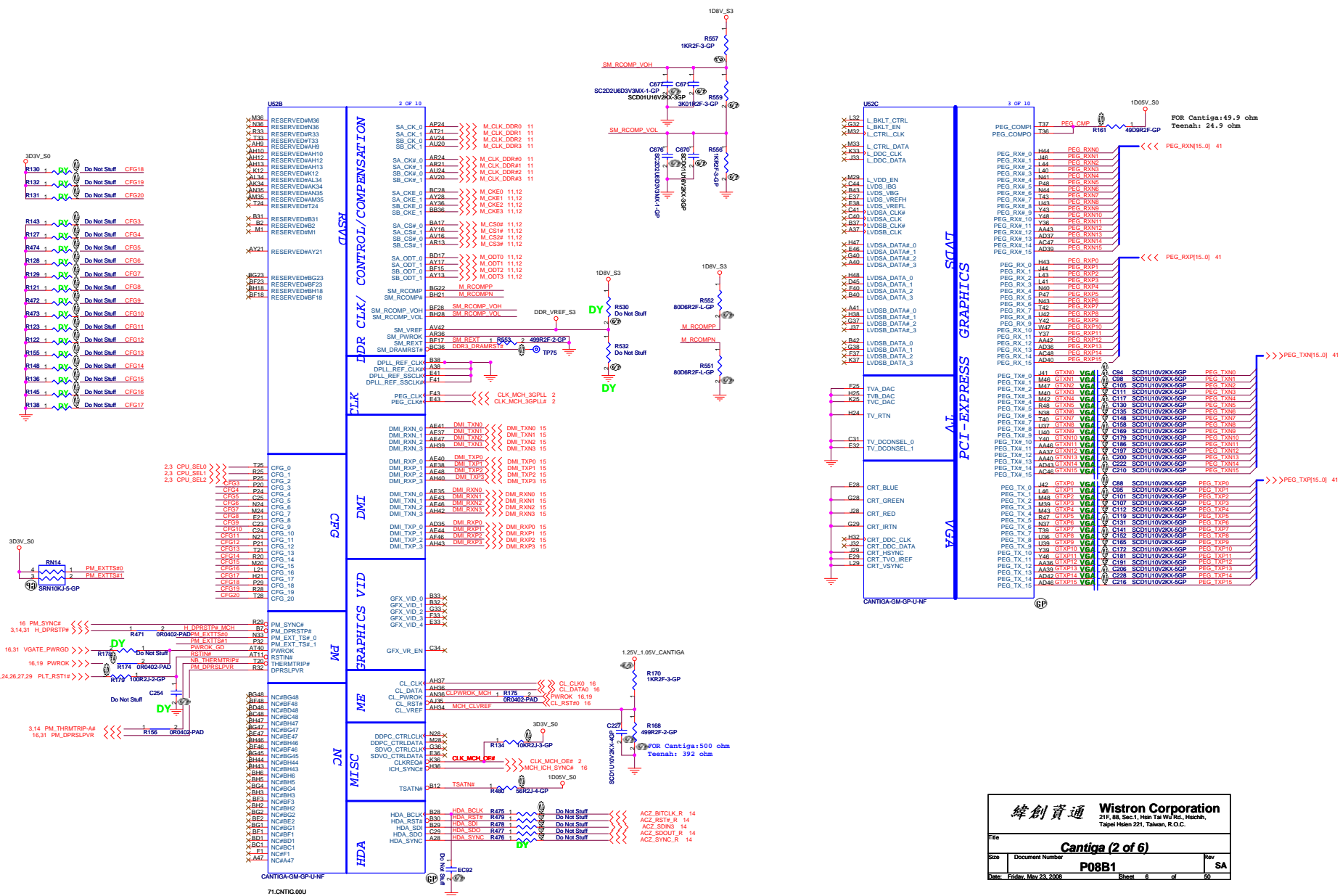
HOST

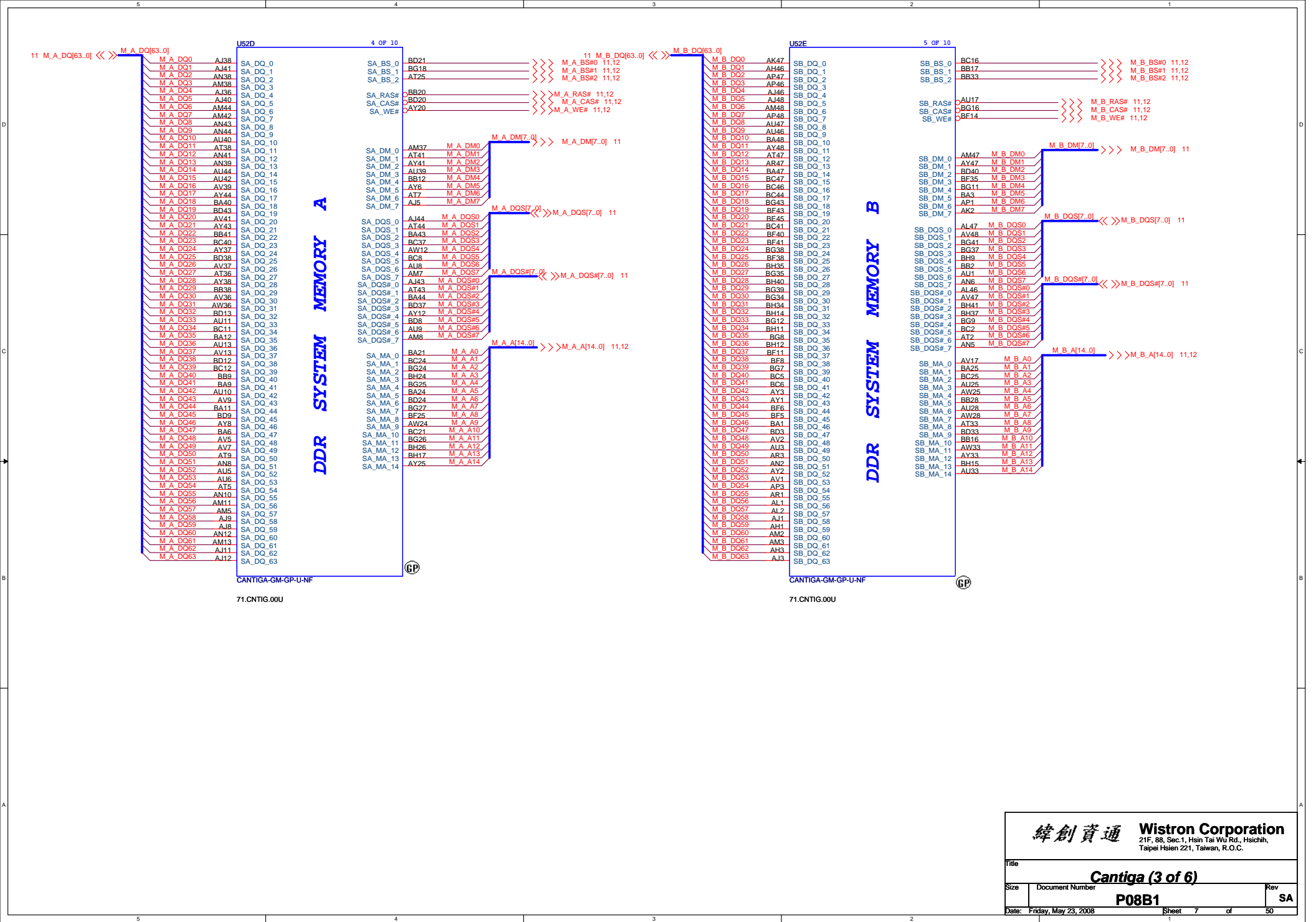
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H_A#_4 C15 H_A#4
H_A#_5 F16 H_A#5
H_A#_6 H13 H_A#6
H_A#_7 C18 H_A#7
H_A#_8 M16 H_A#8
H_A#_9 J13 H_A#9
H_A#_10 P16 H_A#10
H_A#_11 R16 H_A#11
H_A#_12 N17 H_A#12
H_A#_13 M13 H_A#13
H_A#_14 E17 H_A#14
H_A#_15 P17 H_A#15
H_A#_16 G20 H_A#16
H_A#_17 B19 H_A#17
H_A#_18 J16 H_A#18
H_A#_19 E20 H_A#19
H_A#_20 J16 H_A#20
H_A#_21 J20 H_A#21
H_A#_22 L17 H_A#22
H_A#_23 A17 H_A#23
H_A#_24 B17 H_A#24
H_A#_25 L16 H_A#25
H_A#_26 C21 H_A#26
H_A#_27 J17 H_A#27
H_A#_28 H20 H_A#28
H_A#_29 B19 H_A#29
H_A#_30 K17 H_A#30
H_A#_31 B20 H_A#31
H_A#_32 F21 H_A#32
H_A#_33 K21 H_A#33
H_A#_34 L20 H_A#34
H_A#_35
H_ADS# H12 H_ADS# 3
H_ADSTB#_0 B16 H_ADSTB#0 3
H_ADSTB#_1 G17 H_ADSTB#1 3
H_BNR# A2 H_BNR# 3
H_BPR# E11 H_BPR# 3
H_BREQ# G12 H_BREQ#0 3
H_DEFER# E9 H_DEFER# 3
H_DBSY# B10 H_DBSY# 3
HPLL_CLK# AH7 CLK_MCH_BCLK 2
H_DPWR# AH6 CLK_MCH_BCLK# 2
H_DRDY# J11 H_DPWR# 3
H_DRDY# E9 H_DRDY# 3
H_HIT# C9 H_HIT# 3
H_HITM# H11 H_HITM# 3
H_LOCK# H11 H_LOCK# 3
H_TRDY# C9 H_TRDY# 3
H_DINV#_0 J8 H_DINV#0
H_DINV#_1 L3 H_DINV#1
H_DINV#_2 Y13 H_DINV#2
H_DINV#_3 Y1 H_DINV#3
H_DSTBN#_0 L10 H_DSTBN#0
H_DSTBN#_1 J17 H_DSTBN#1
H_DSTBN#_2 A15 H_DSTBN#2
H_DSTBN#_3 AE6 H_DSTBN#3
H_DSTBP#_0 L9 H_DSTBP#0
H_DSTBP#_1 M8 H_DSTBP#1
H_DSTBP#_2 AA6 H_DSTBP#2
H_DSTBP#_3 AE5 H_DSTBP#3
H_REQ#_0 B15 H_REQ#0
H_REQ#_1 K13 H_REQ#1
H_REQ#_2 F13 H_REQ#2
H_REQ#_3 B13 H_REQ#3
H_REQ#_4 B14 H_REQ#4
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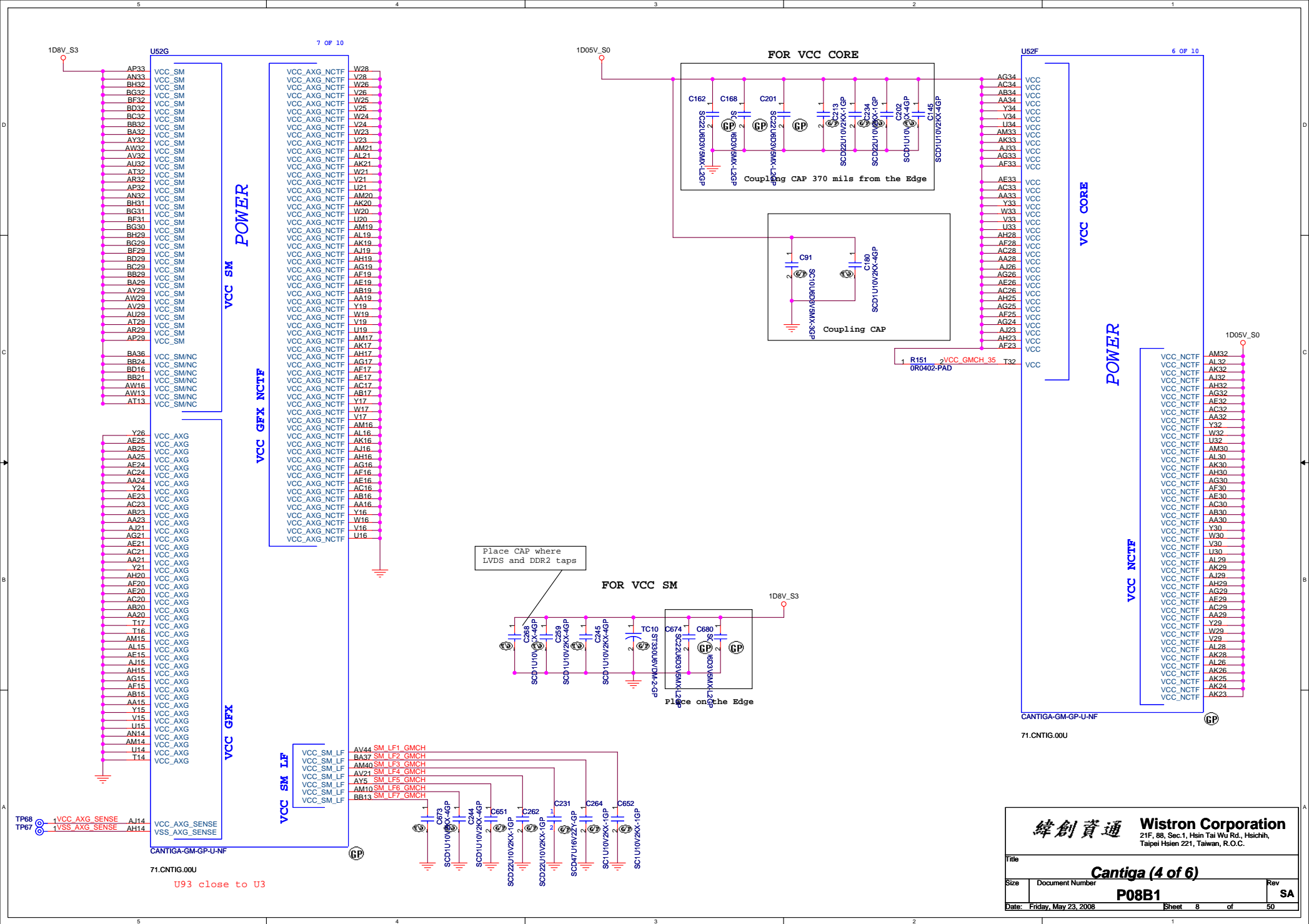
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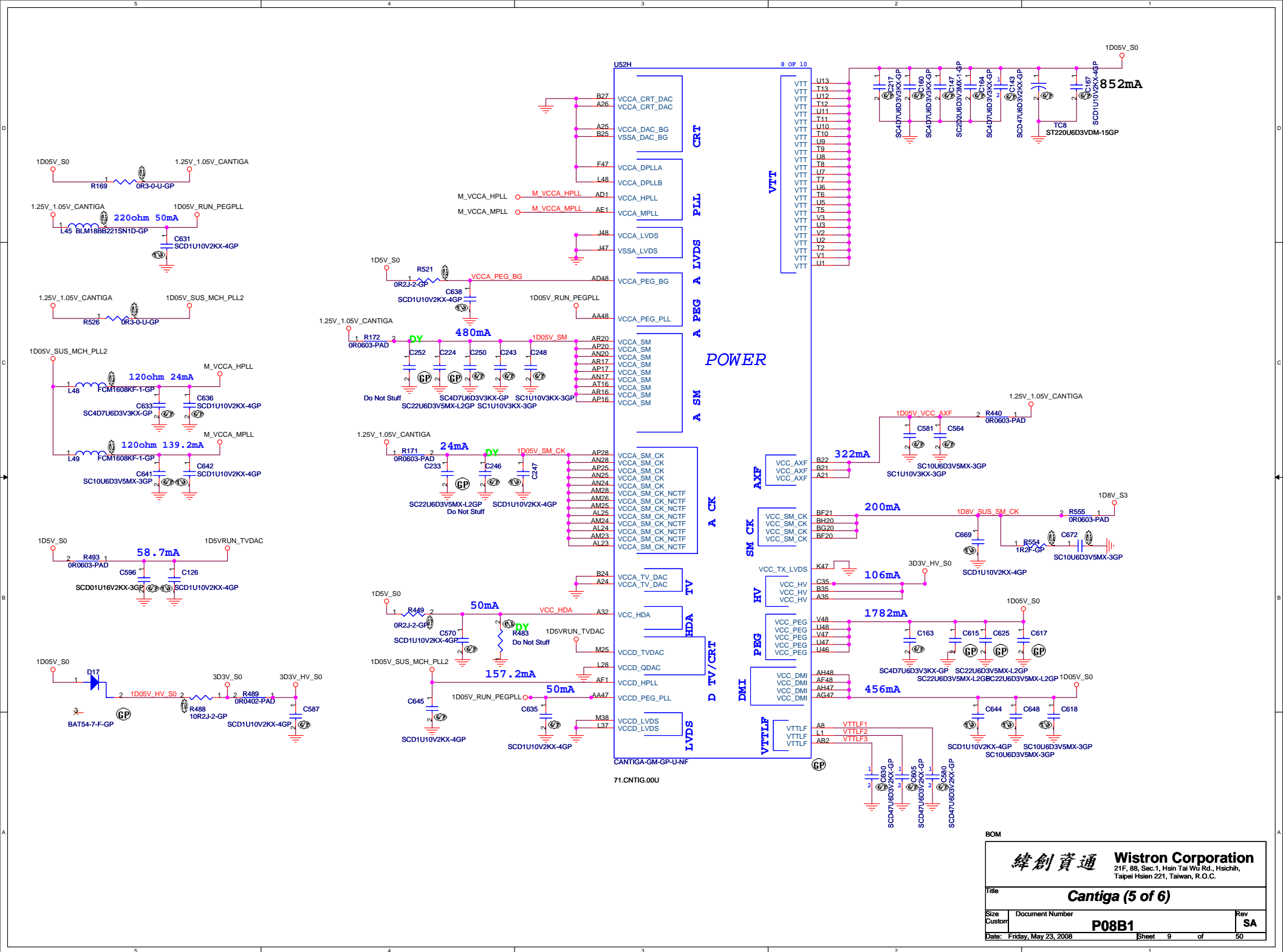
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Size Document Number
Date: Friday, May 23, 2008
Sheet 5 of 50
Rev SA
P08B1



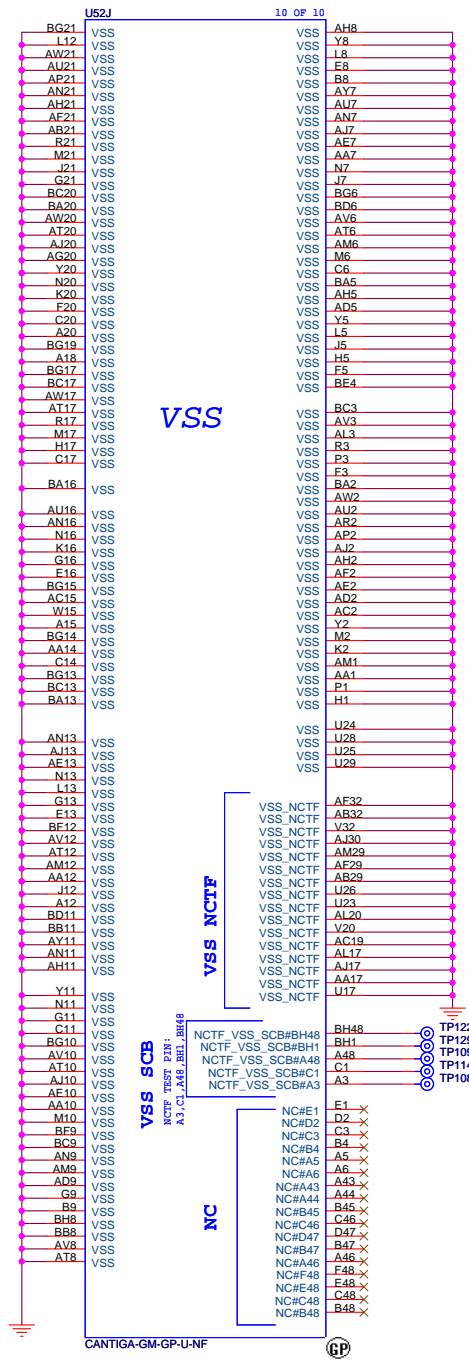
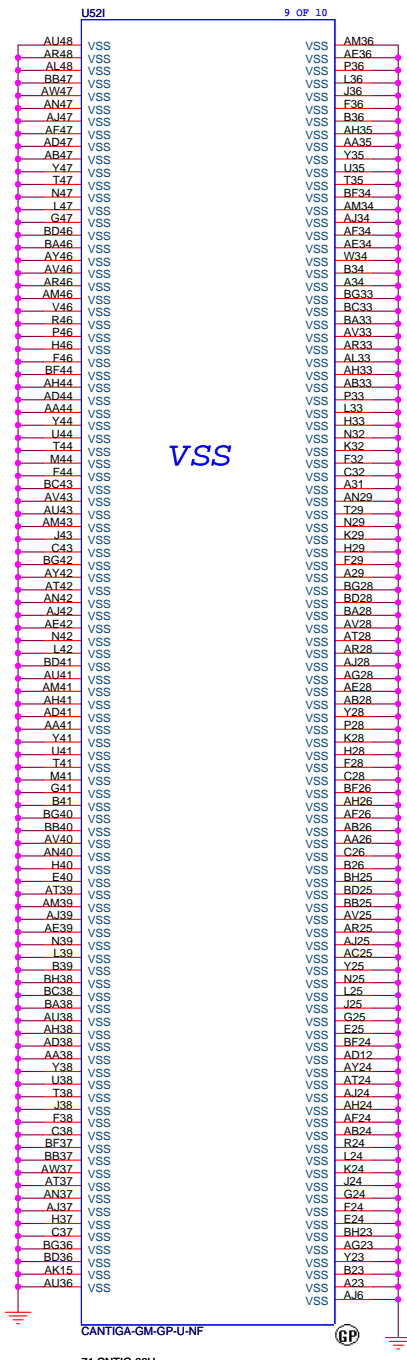






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Title			Cantiga (5 of 6)	
Size	Document Number	P08B1		Rev
Customer				SA
Date:	Friday, May 23, 2008	Sheet	9	of 50



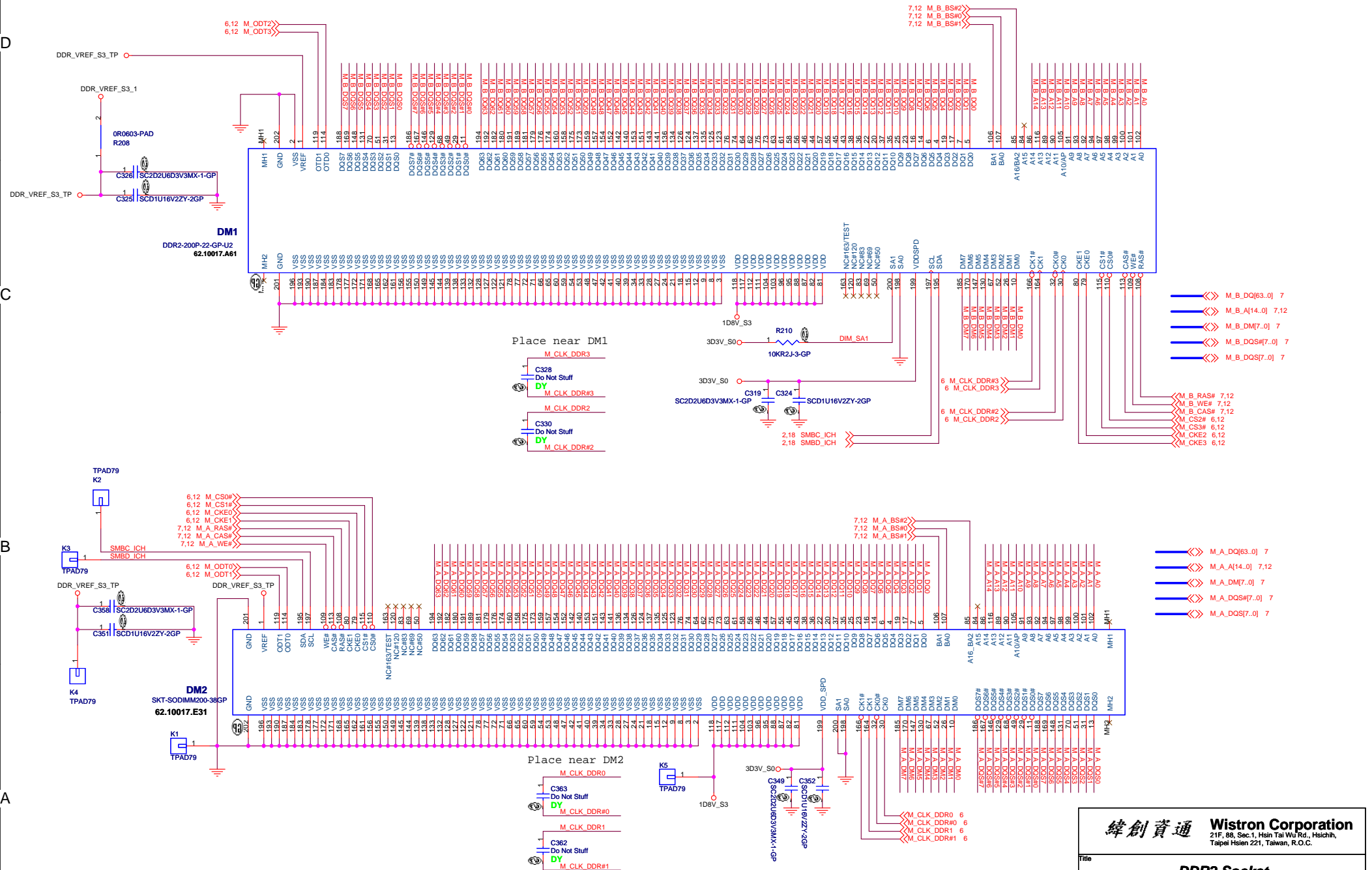
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Title
Cantiga (6 of 6)

Size Document Number Rev
P08B1 SA

Date: Friday, May 23, 2008 Sheet 10 of 50

DDR SOCKET

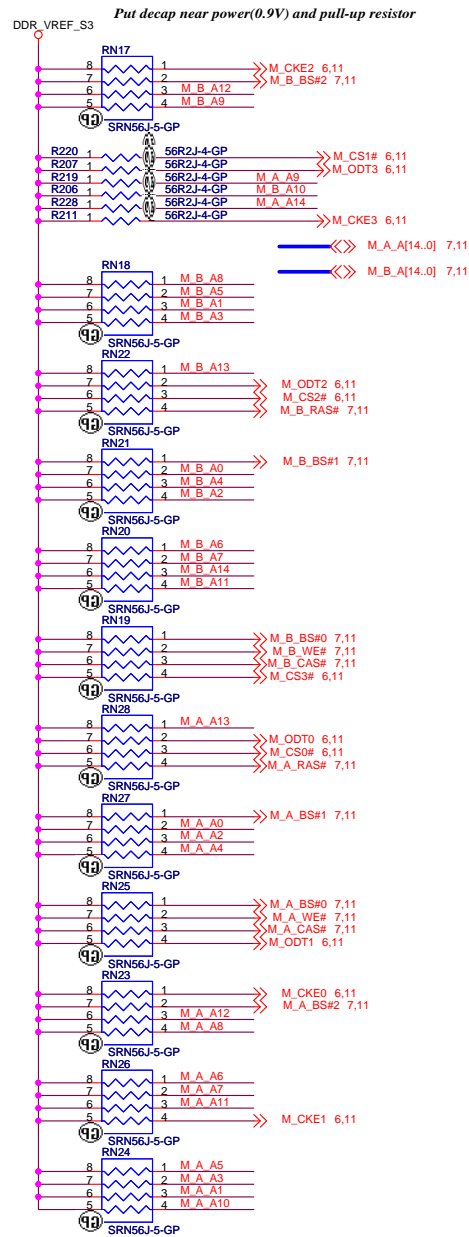


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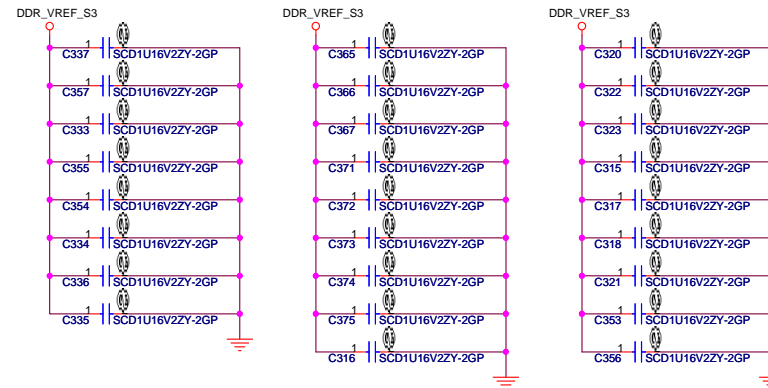
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DDR2 Socket			
Size	Document Number		Rev
	P08B1		SA
Date:	Friday, May 23, 2008		Sheet 11 of 50

PARALLEL TERMINATION

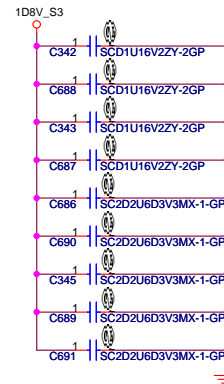
Decoupling Capacitor



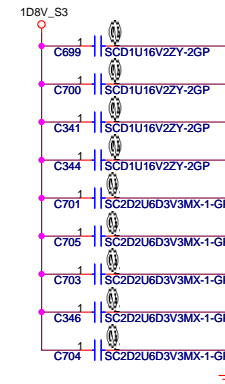
Put decap near power(0.9V) and pull-up resistor

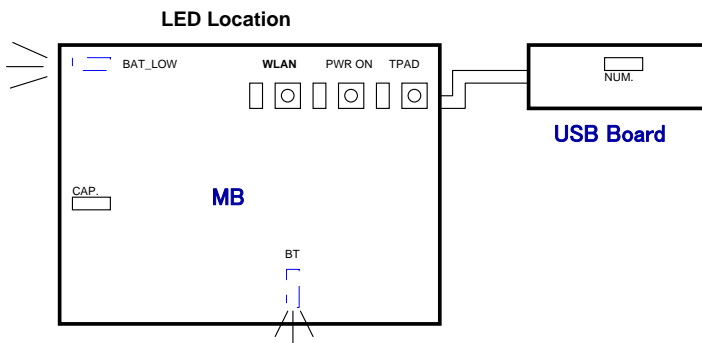
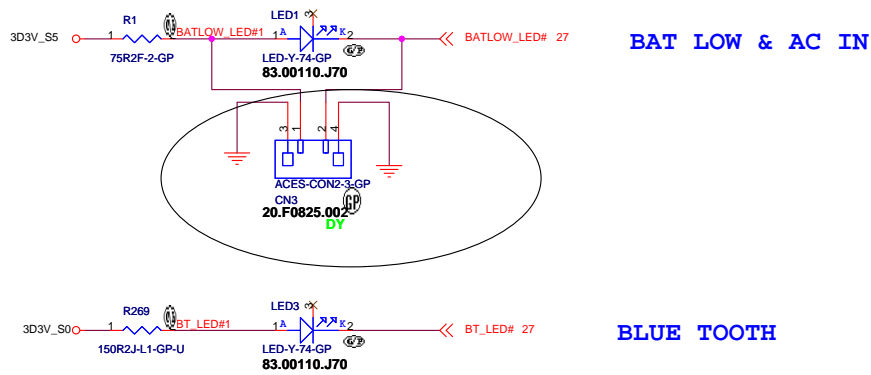
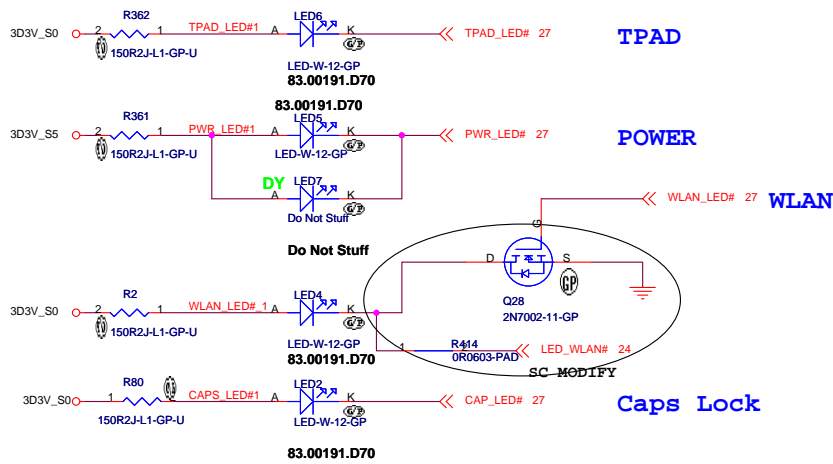


Place these Caps near DM1

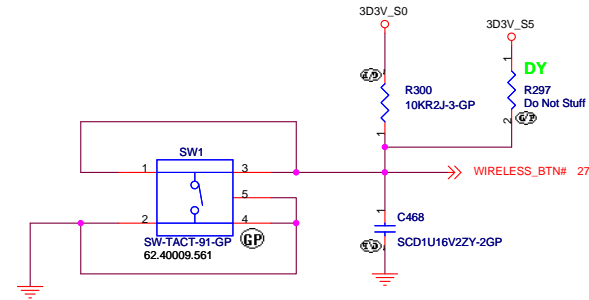


Place these Caps near DM2

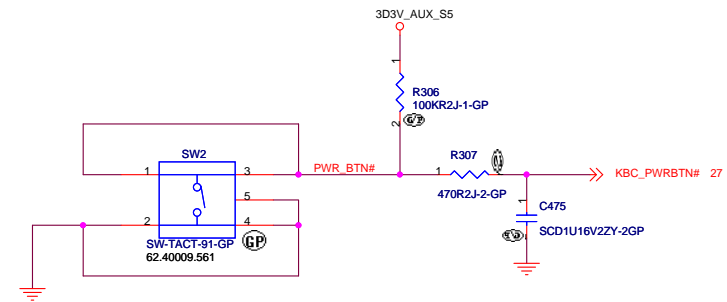




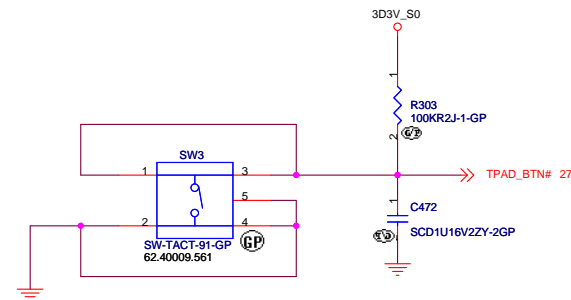
WIRELESS BUTTON & LED



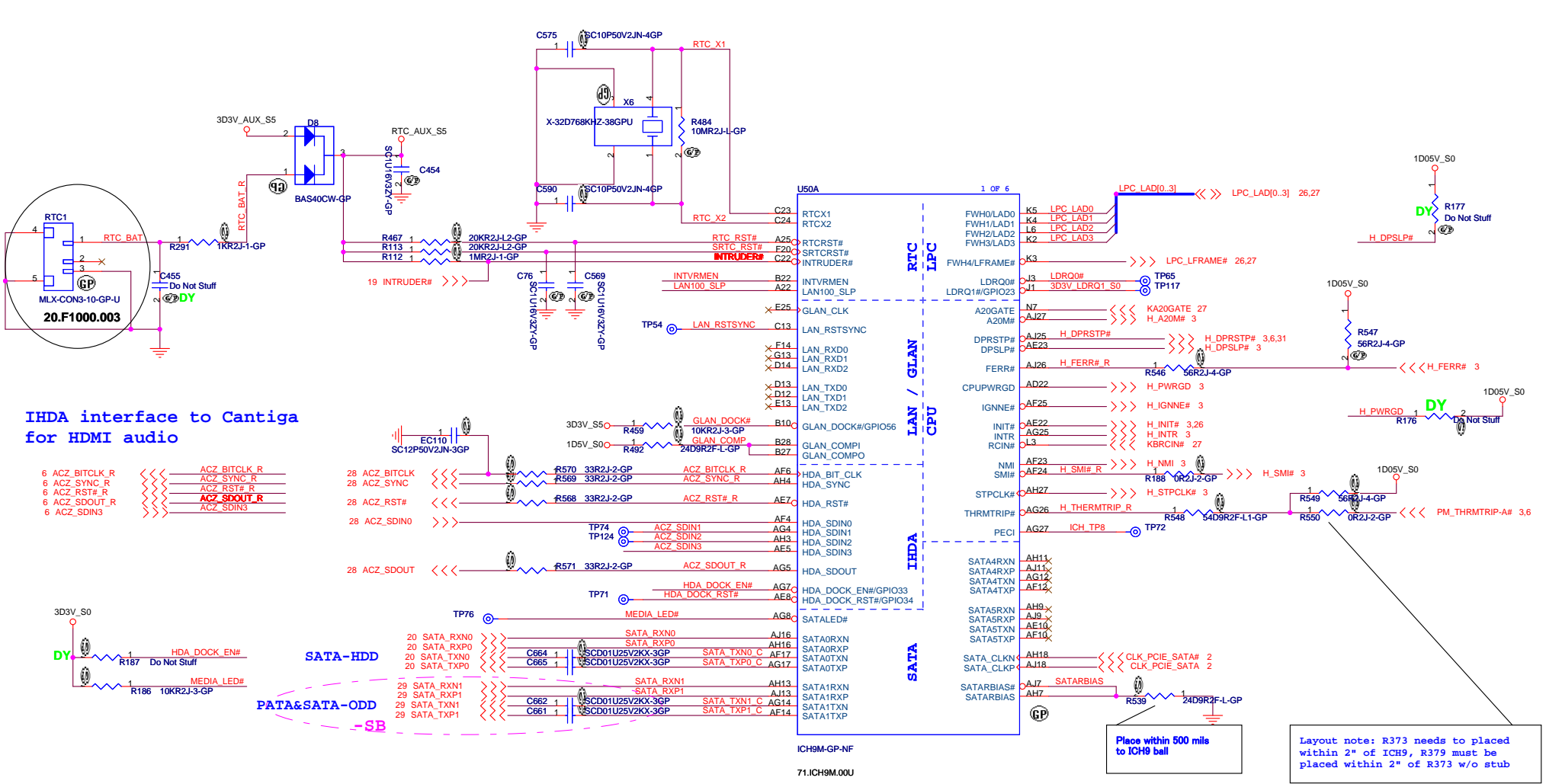
POWER BUTTON & LED



TPAD BUTTON & LED



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Title			
LED / SW			
Size	Document Number		Rev
	P08B1		SA
Date:	Friday, May 23, 2008	Sheet 13 of 50	



IHDA interface to Cantiga
for HDMI audio

- 6 ACZ_BITCLK_R <<< ACZ_BITCLK_R
- 6 ACZ_SYNC_R <<< ACZ_SYNC_R
- 6 ACZ_RST#_R <<< ACZ_RST#_R
- 6 ACZ_SDOUT_R <<< ACZ_SDOUT_R
- 6 ACZ_SDIN3 <<< ACZ_SDIN3

SATA-HDD

PATA&SATA-ODD
-SB

Integrated VccSus1_05,VccSus1_5,VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
Integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

Place within 500 mils
to ICH9 ball

Layout note: R373 needs to be placed
within 2" of ICH9, R379 must be
placed within 2" of R373 w/o stub

緯創資通

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Title

ICH9-M (1 of 5)

Size

Document Number

Rev

P08B1

SA

Date: Friday, May 23, 2008

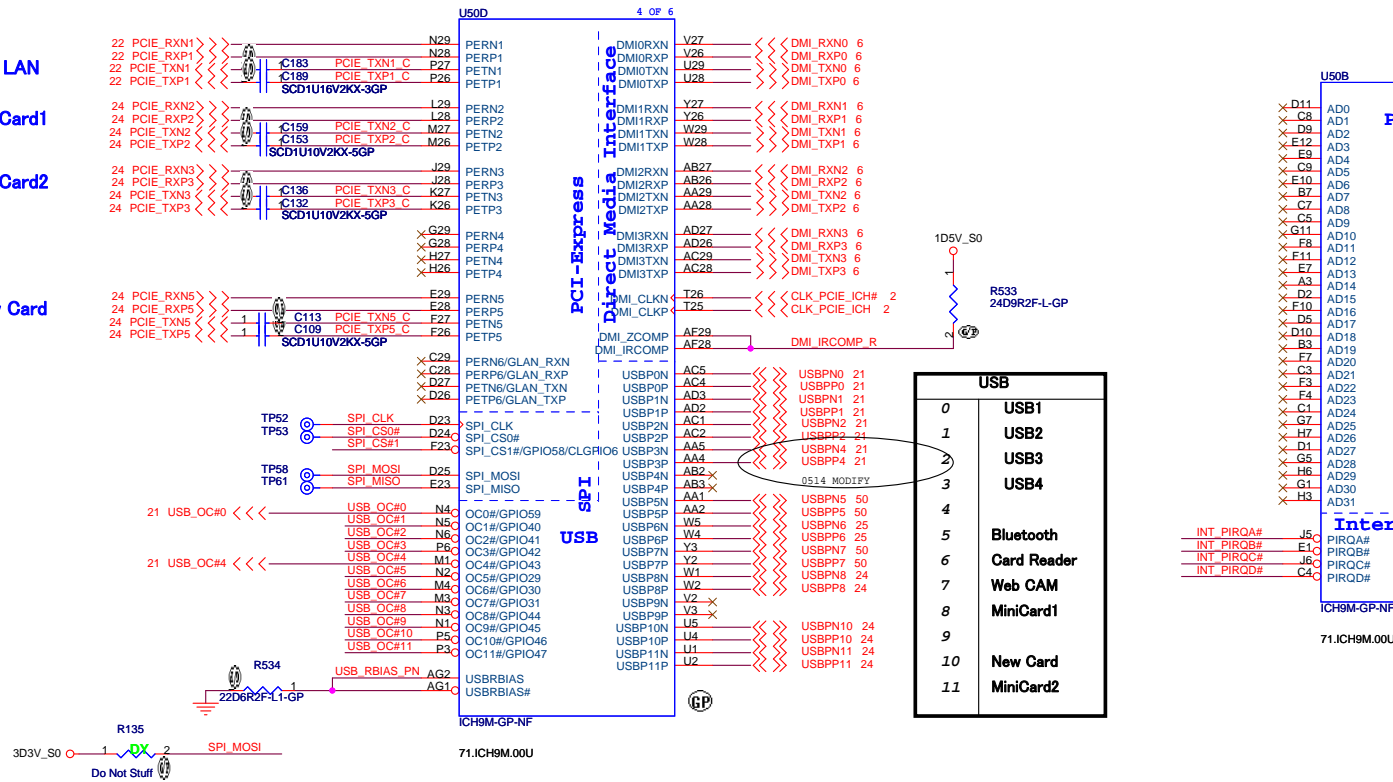
Sheet 14 of 50

LAN

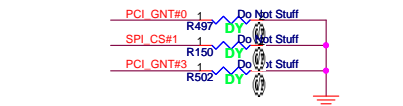
MiniCard1

MiniCard2

New Card



BOOT BIOS Strap		
PCI_GNT#0	SPI_CS#1	BOOT BIOS Location
0	1	SPT
1	0	PCI
1	1	LPC(Default)
A16 swap override strap		
PCI_GNT#3	Low = A16 swap override enable high = default	



BOM

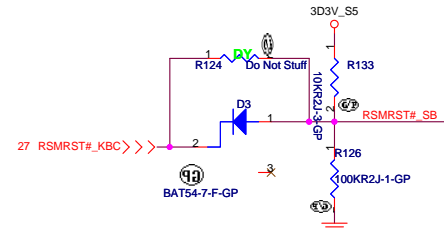
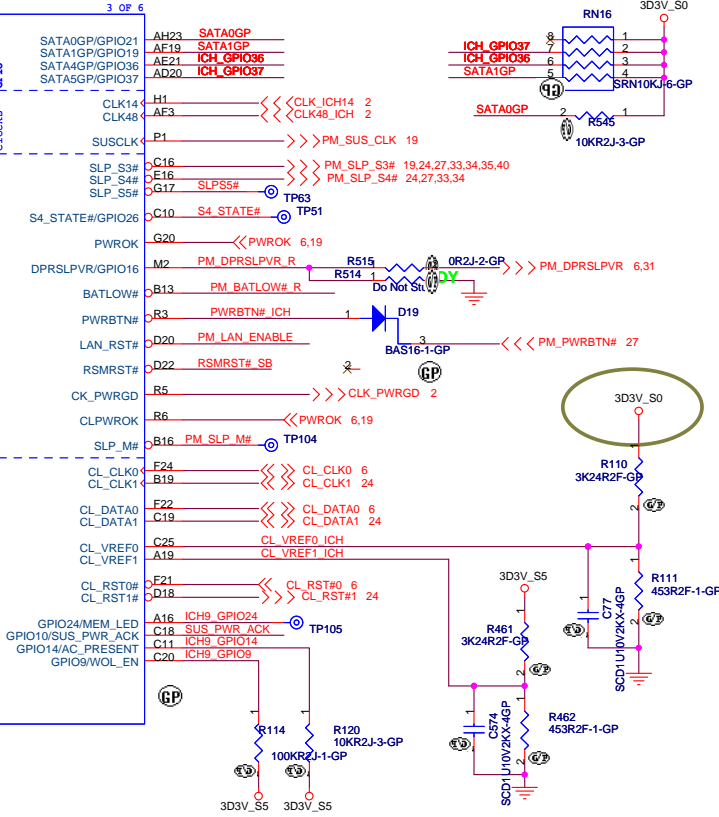
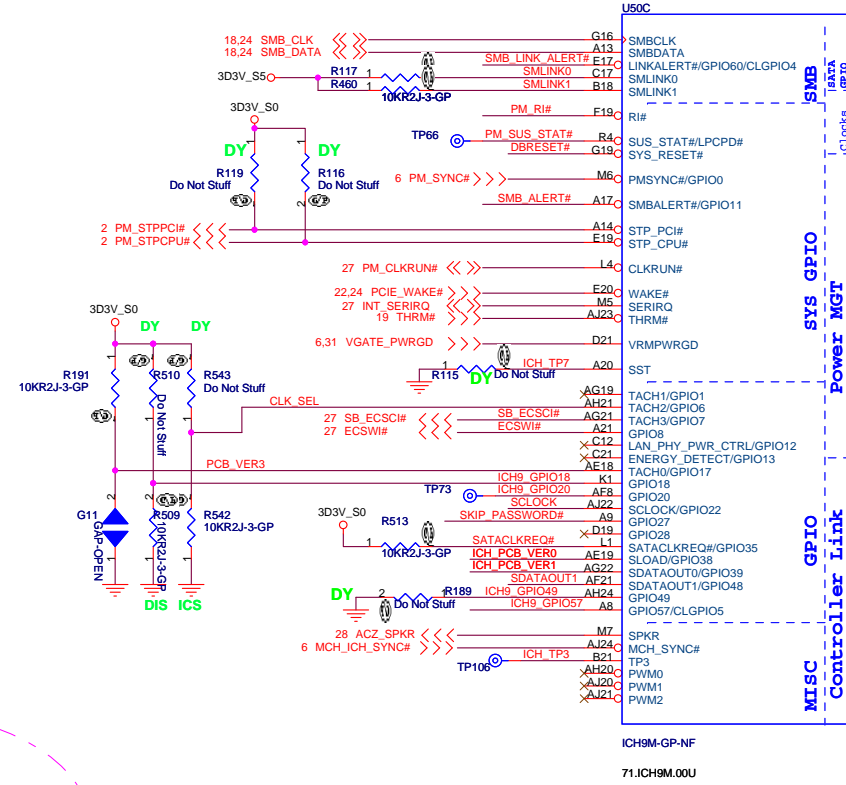
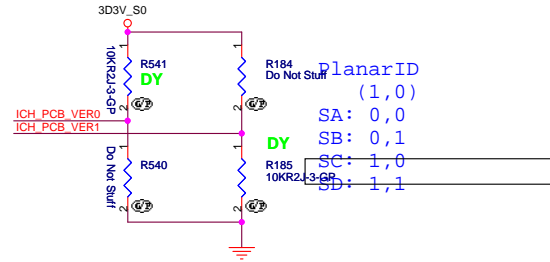
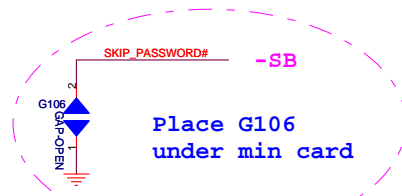
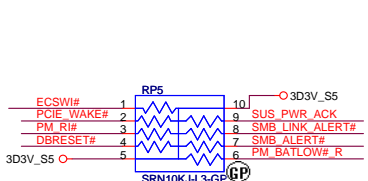
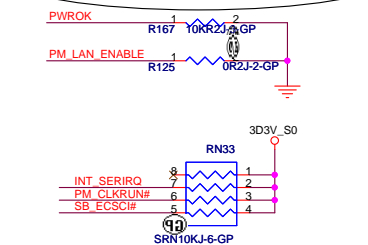
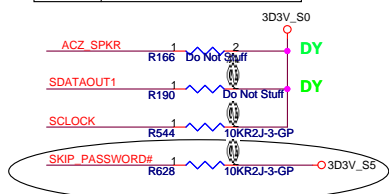
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Title **ICH9-M (2 of 5)**

Size Document Number **P08B1** Rev SA

Date: Friday, May 23, 2008 Sheet 15 of 50

No Reboot Strap	
SPKR	LOW = Default High = No Reboot

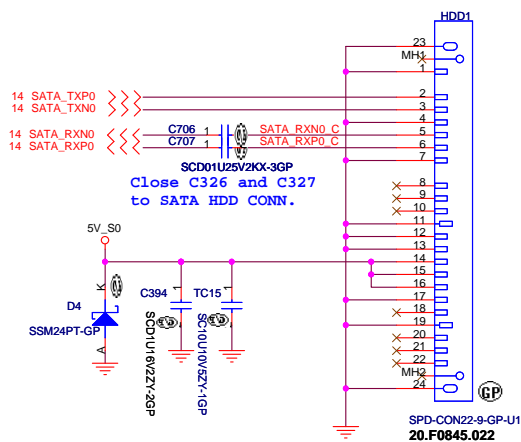


BOM			
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Title ICH9-M (2 of 4)			
Size	Document Number	Rev	SA
P08B1			
Date: Friday, May 23, 2008	Sheet 16	of	50



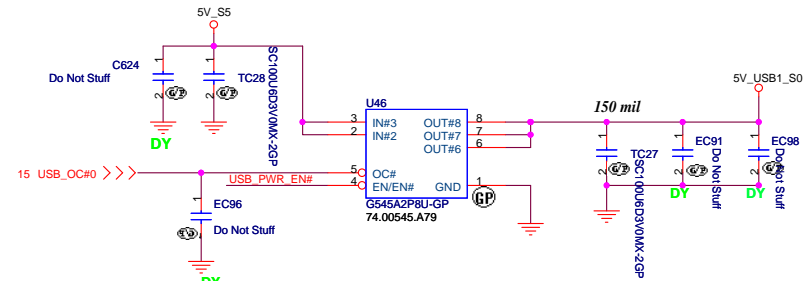
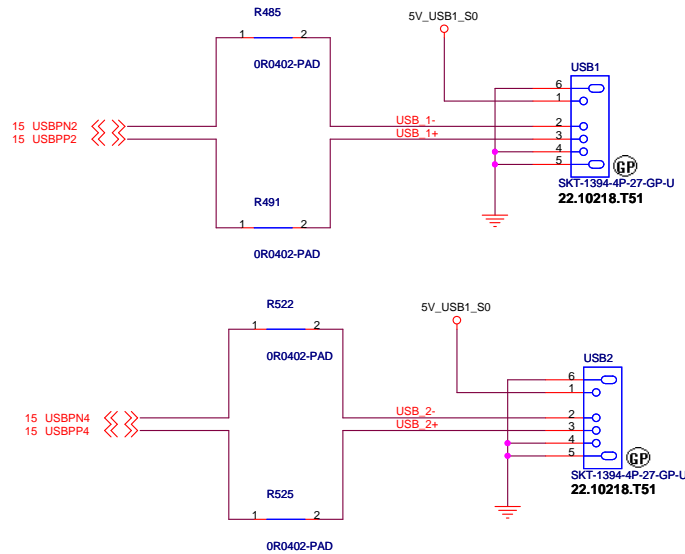
Date: Friday, May 23, 2008	Sheet 18 of 50
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SATA HD Connector

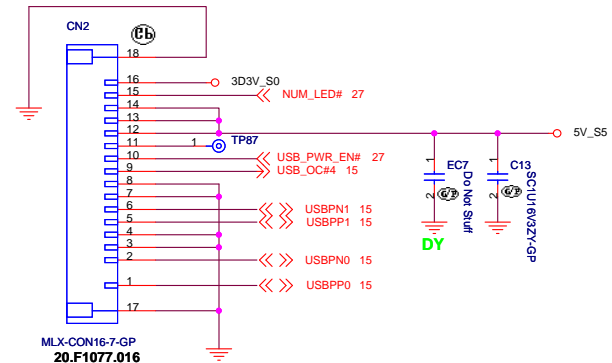


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Title HDD / CDROM / LAUNCH			
Size	Document Number P08B1		Rev SA
Date:	Friday, May 23, 2008	Sheet 20 of	50

USB CONN

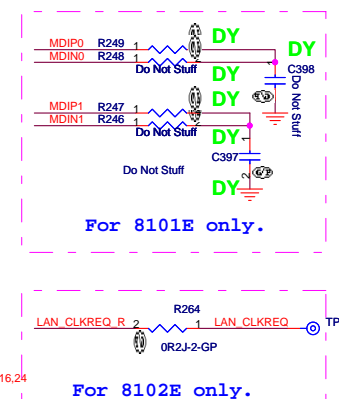
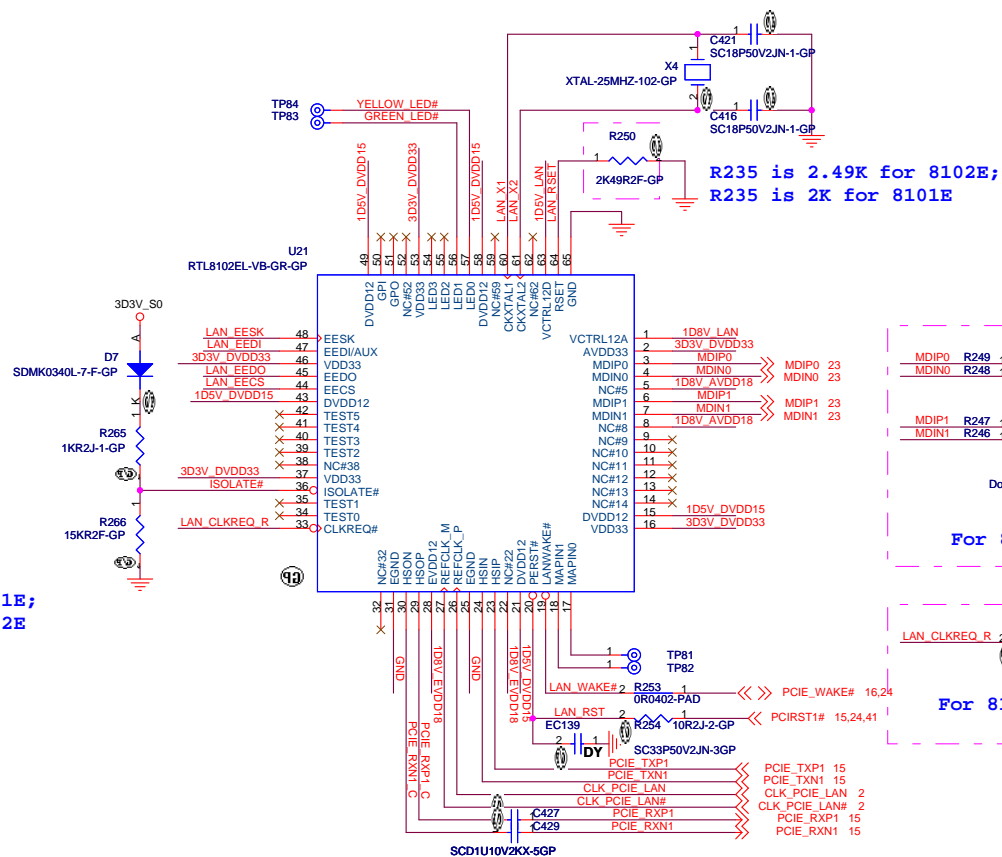
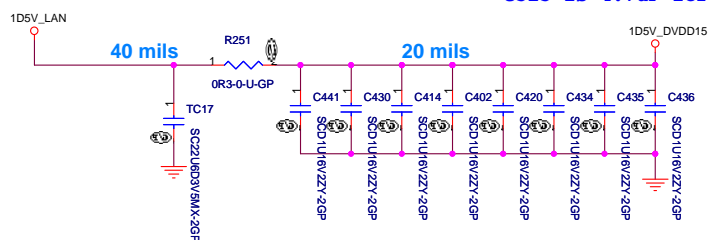
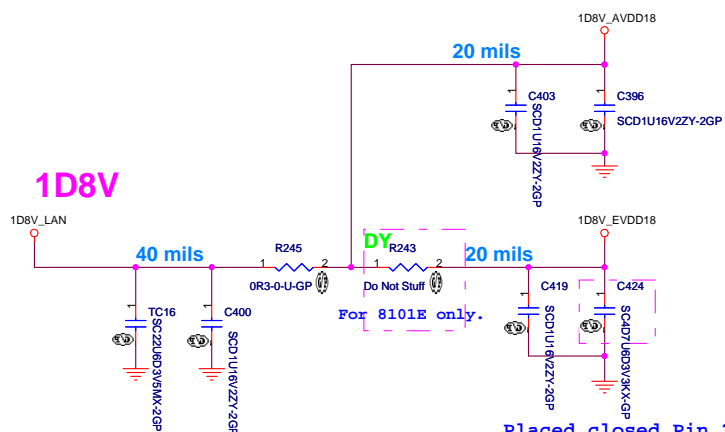
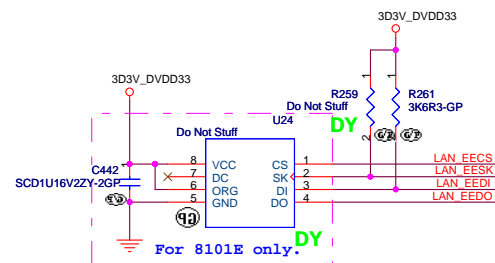
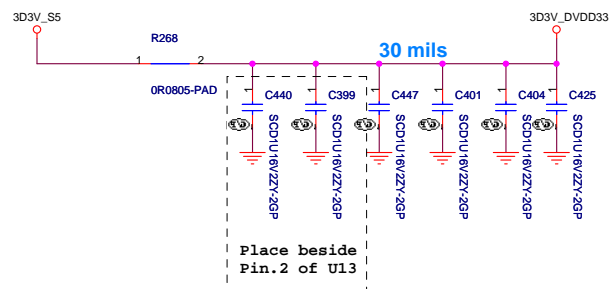


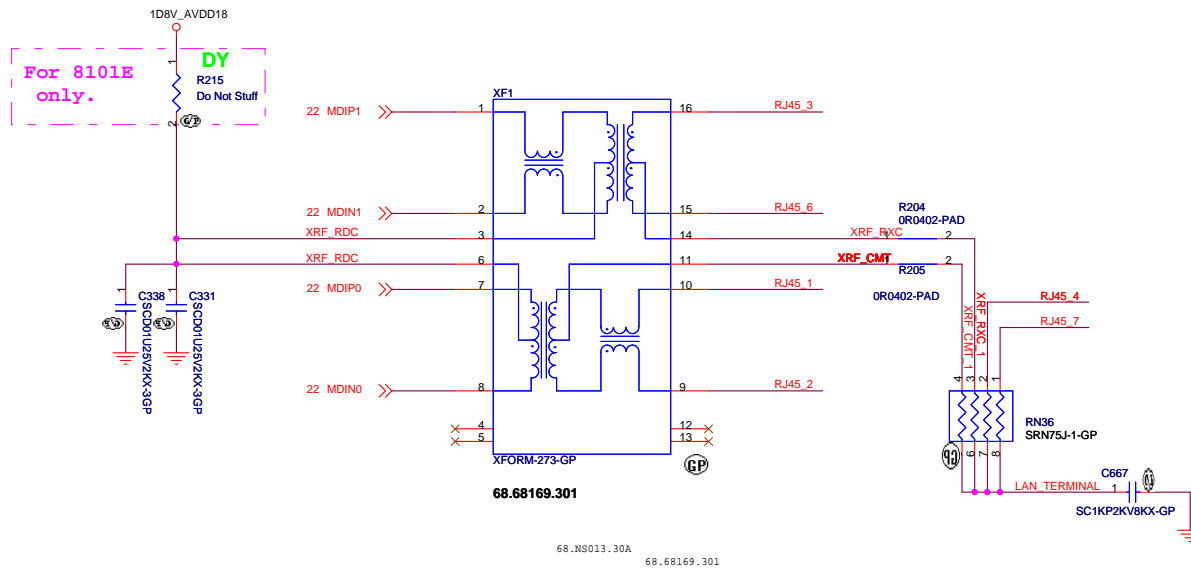
USB Board CONN



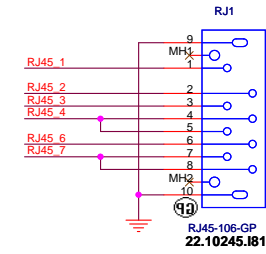
BOM

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
USB / BLUETOOTH			
Size	Document Number		Rev
	P08B1		SA
Date:	Friday, May 23, 2008	Sheet 21 of 50	





LAN Connector

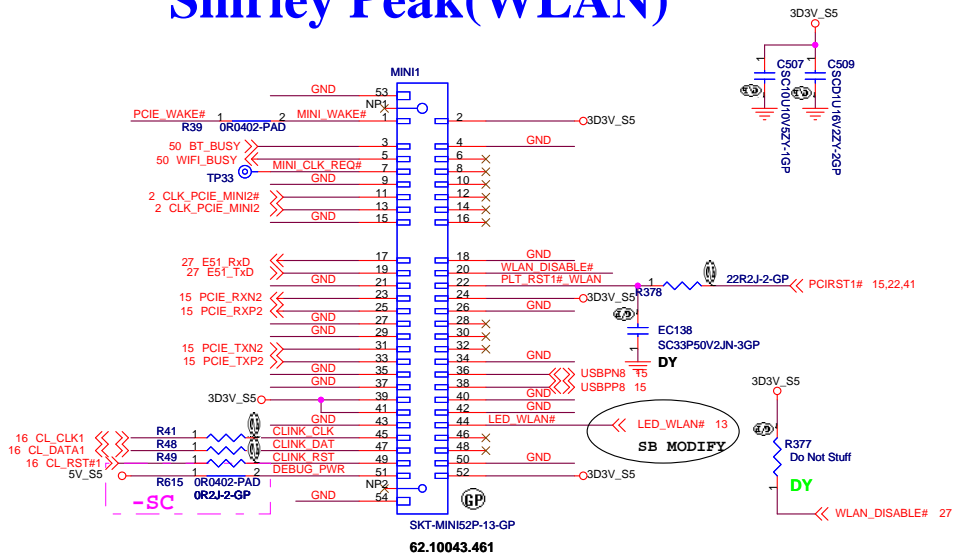


BOM

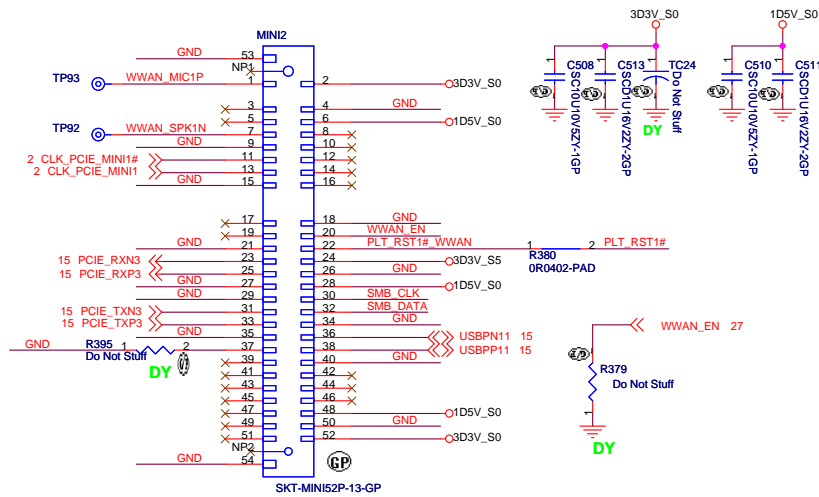
緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		RJ45 LAN CONN	
Size A3	Document Number	P08B1	Rev SA
Date: Tuesday, May 27, 2008		Sheet 23 of 50	

CLOSE TO
TRANSFORMER

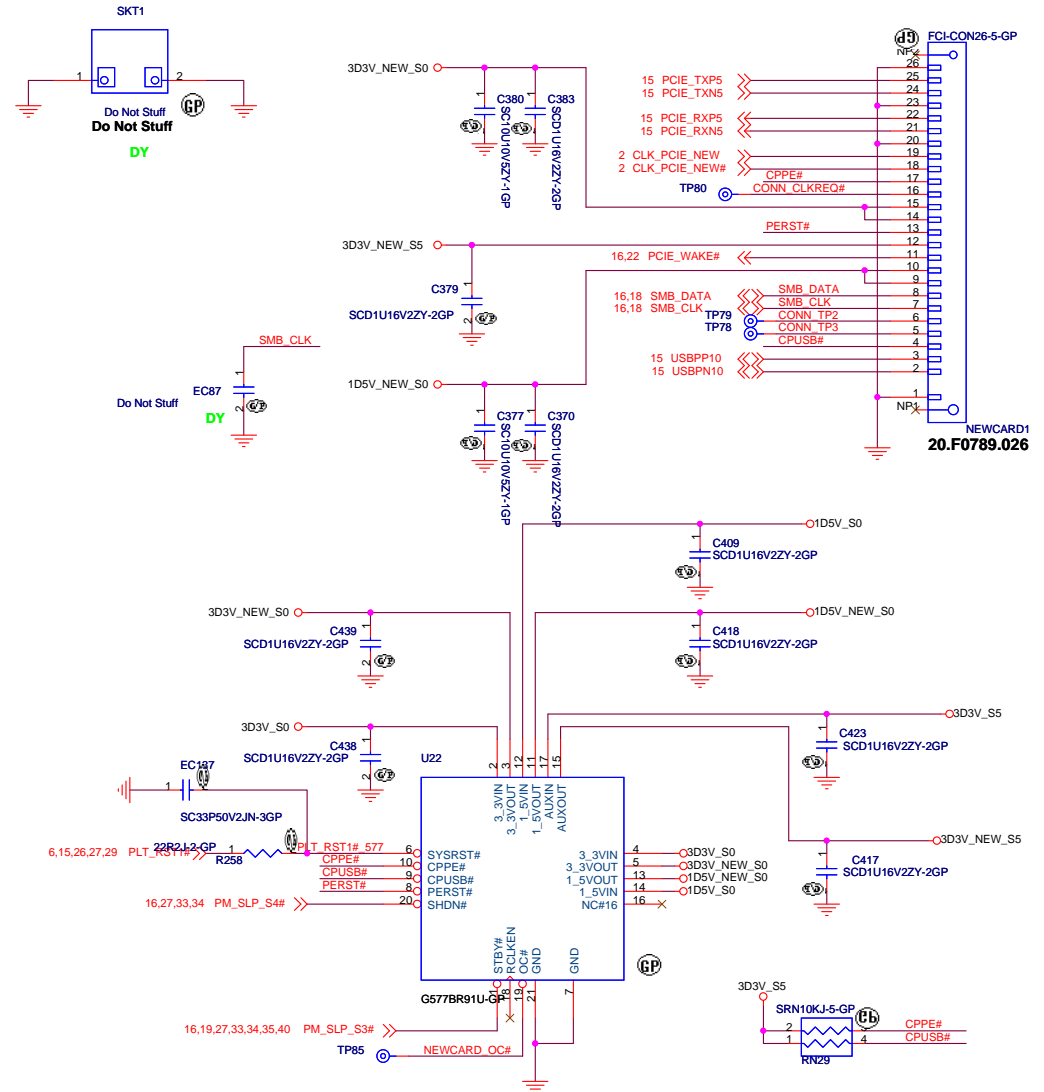
Shirley Peak(WLAN)



ROBSON



New Card

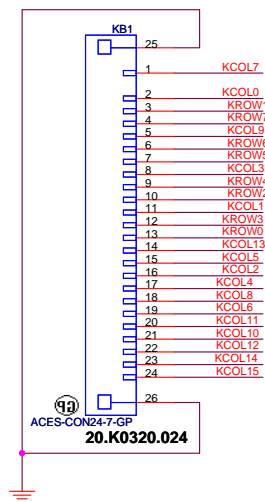


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緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Mini Card/New Card			
Size	Document Number		Rev
	P08B1		SA
Date:	Friday, May 23, 2008	Sheet 24 of 50	

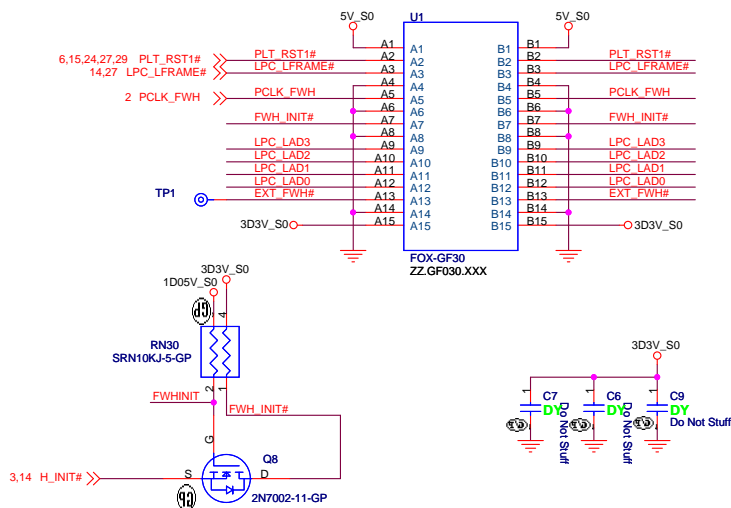
Internal KeyBoard Connector

《KROW[0..7] 27
《KCOL[0..15] 27



GOLDEN FINGER FOR DEBUG BOARD

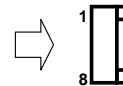
LPC_LAD[0..3] 《 LPC_LAD[0..3] 14,27



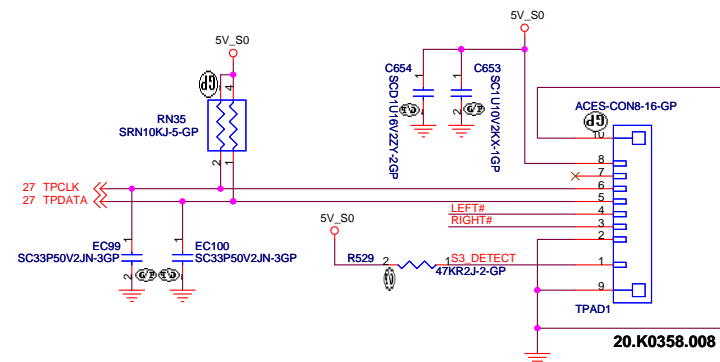
TOP VIEW

A15 (B1)
A14 (B2)
:
:
A2 (B14)
A1 (B15)

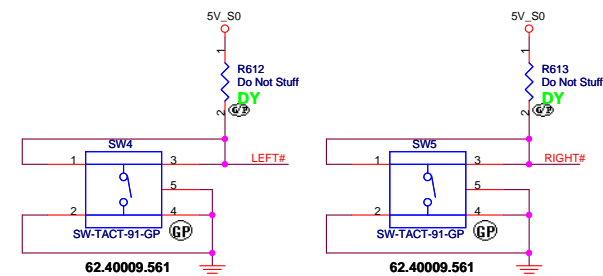
(BOTTOM VIEW)



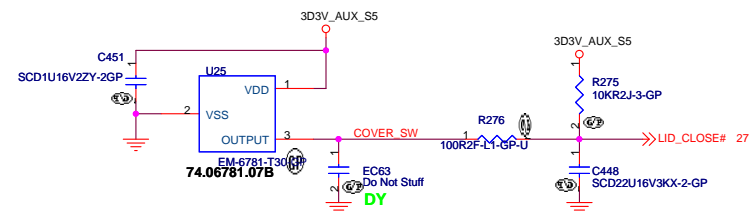
TouchPad Connector



15" TOUCHPAD BUTTON SWITCH

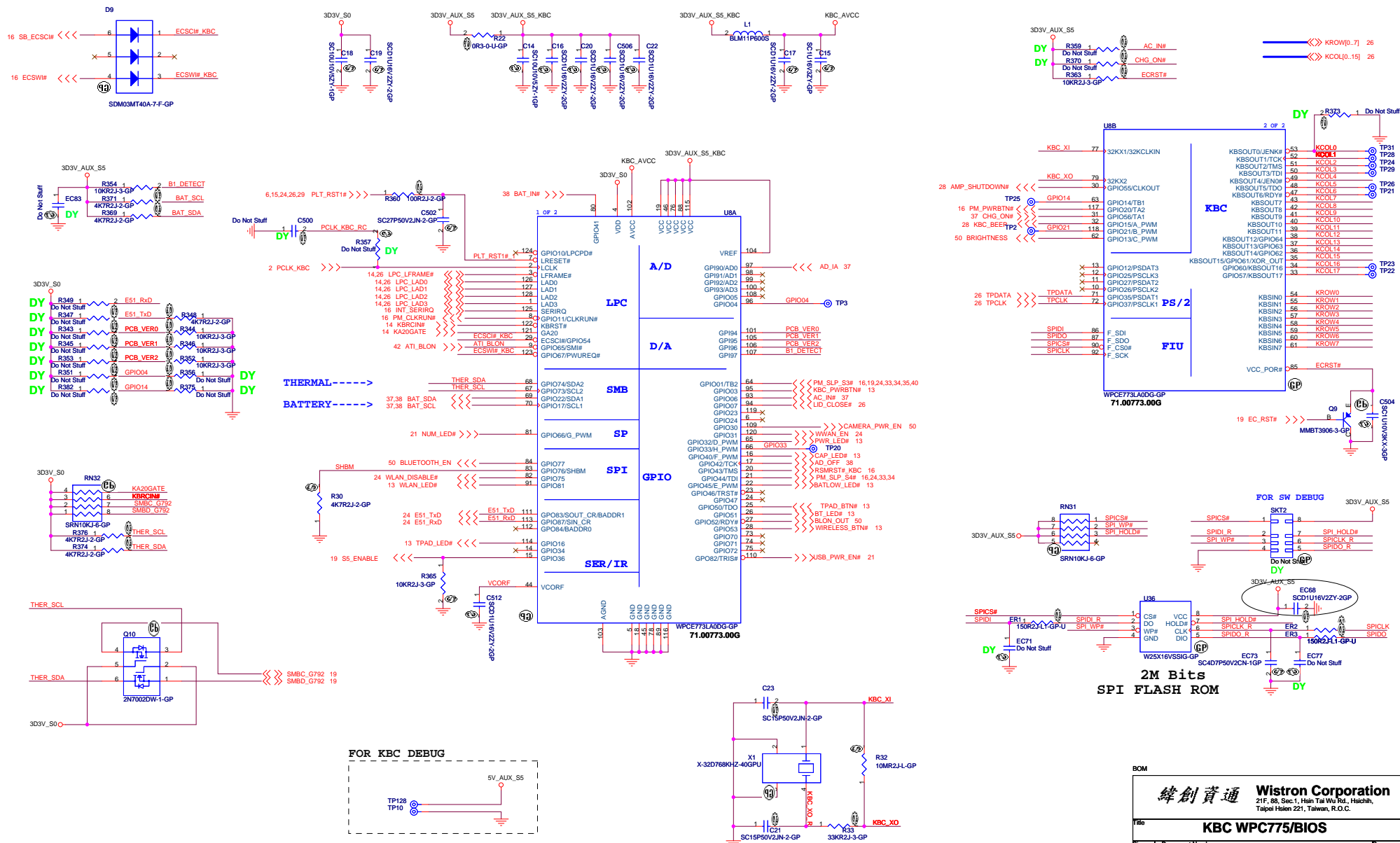


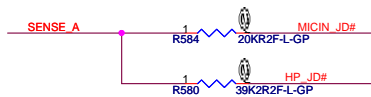
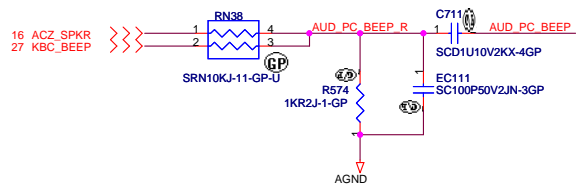
COVER SWITCH



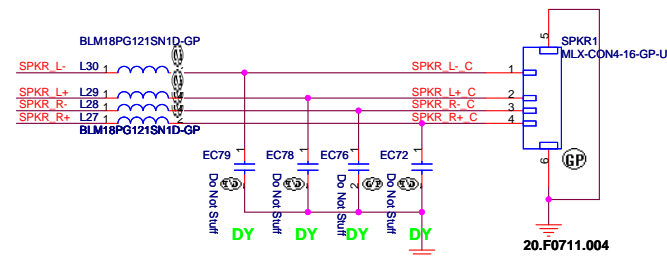
BOM

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
KeyBoard/TPAD/Debug			
Size	Document Number		Rev
Custom		P08B1	SA
Date:	Friday, May 23, 2008	Sheet	26 of 50

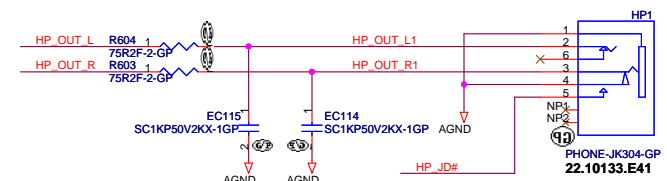




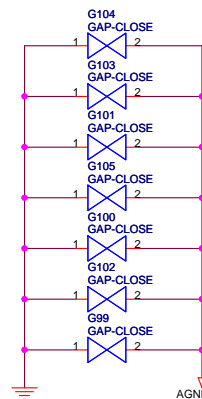
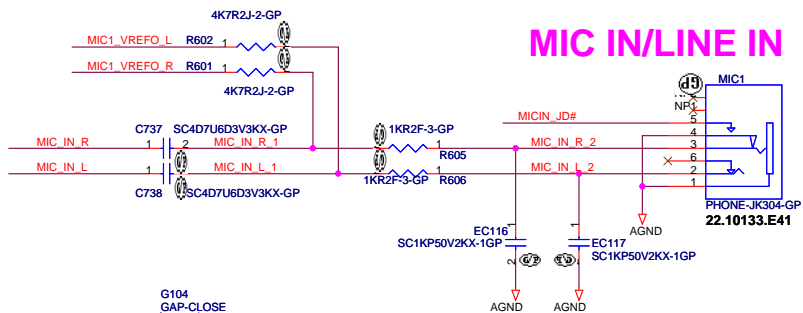
Internal Speaker 1.5W x 2



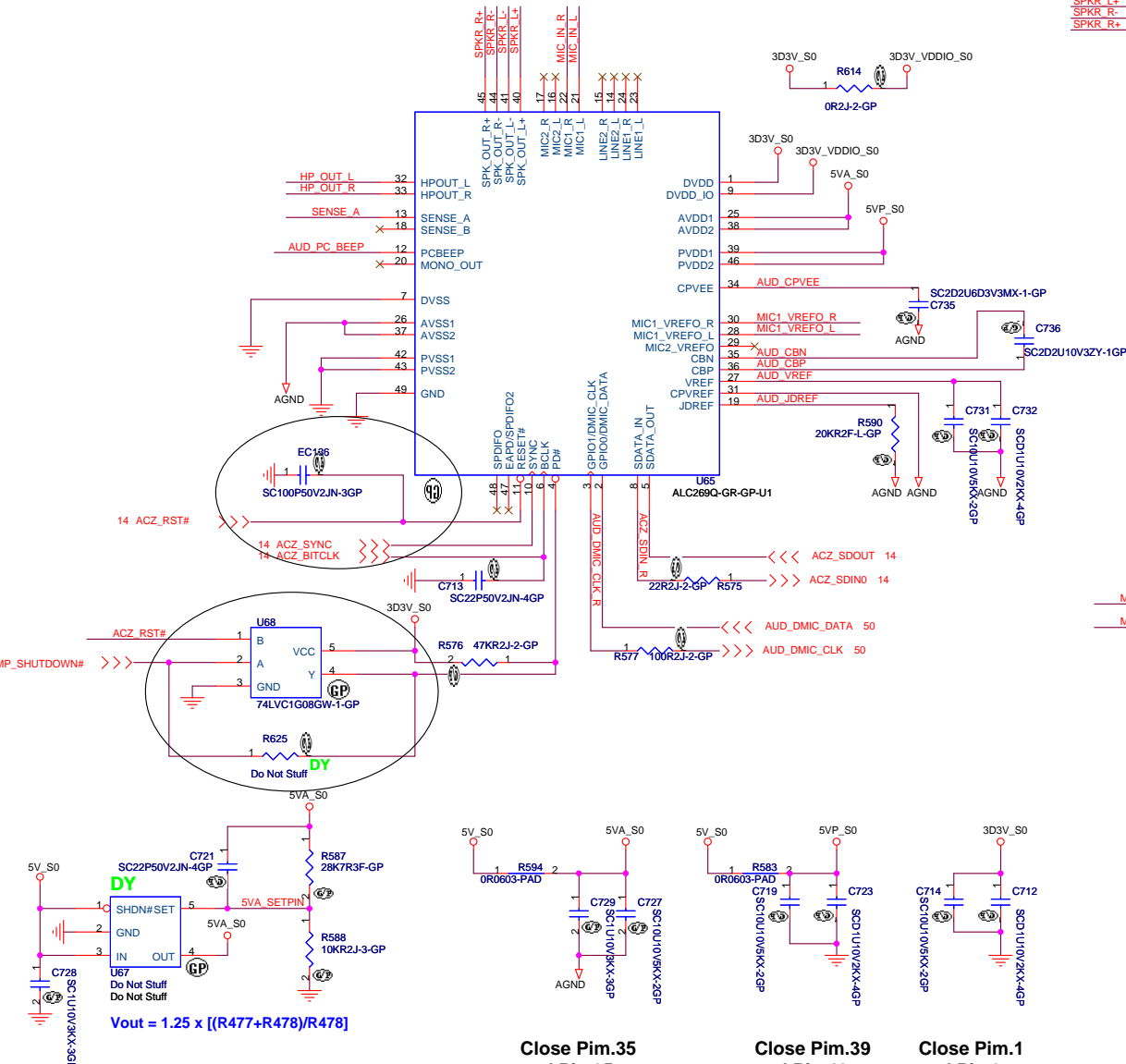
Headphone OUT



MIC IN/LINE IN



BOM		緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title		ALC269 / AUDIO JACK	
Size A3	Document Number	P08B1	Rev SA
Date: Friday, May 23, 2008		Sheet 28	of 50

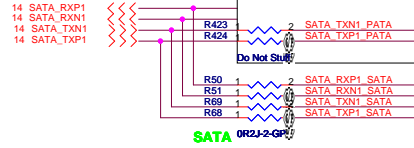
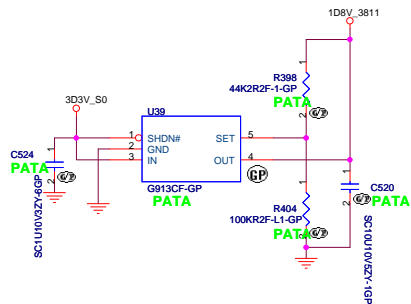


Close Pim.35 and Pin.35

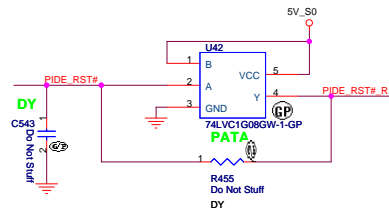
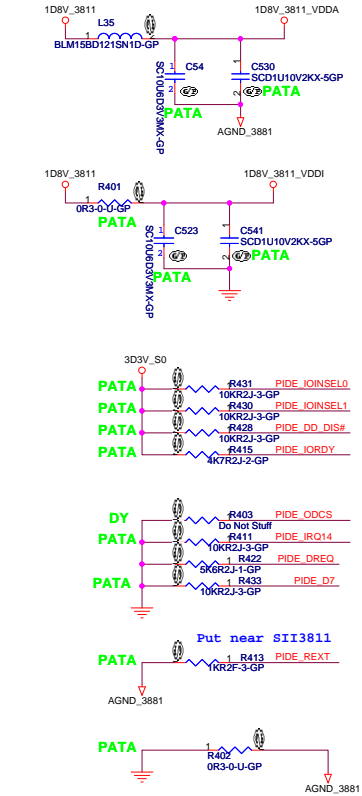
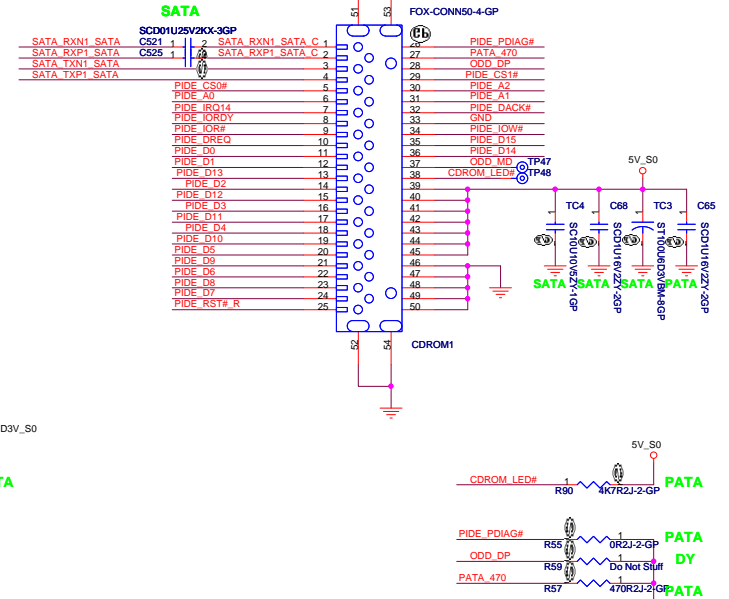
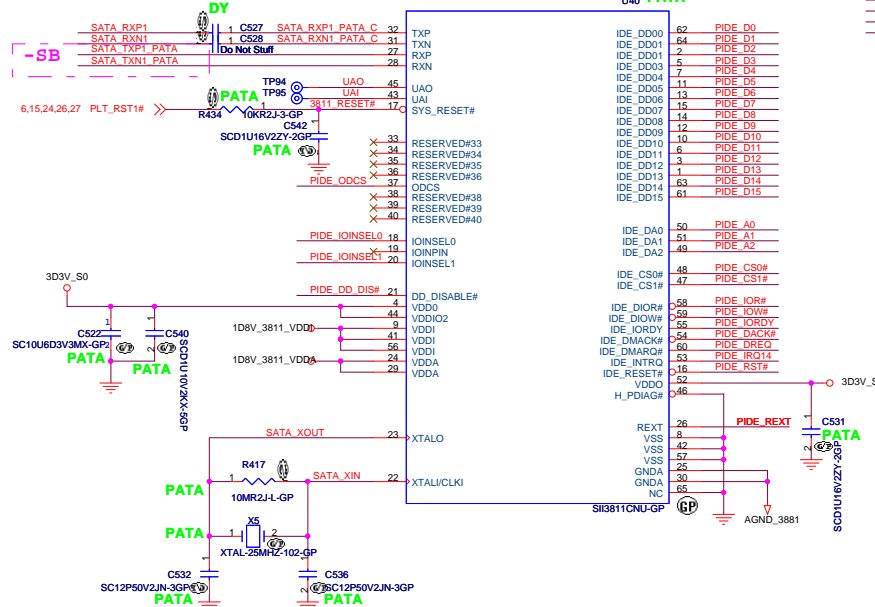
Close Pim.39 and Pin.46

Close Pim.1 and Pin.9

$$V_{out} = 1.25 \times [(R477+R478)/R478]$$

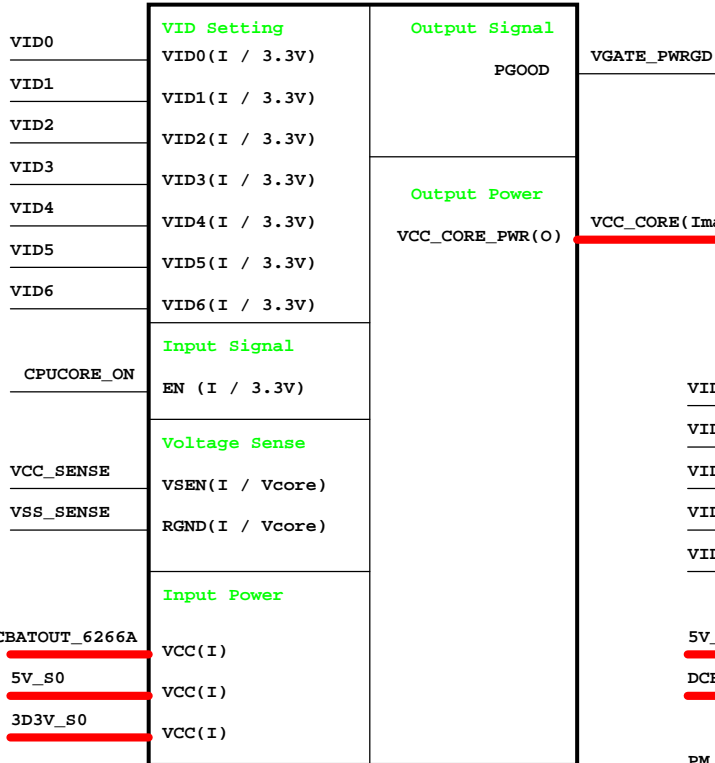


Sil3811 SATA to PATA

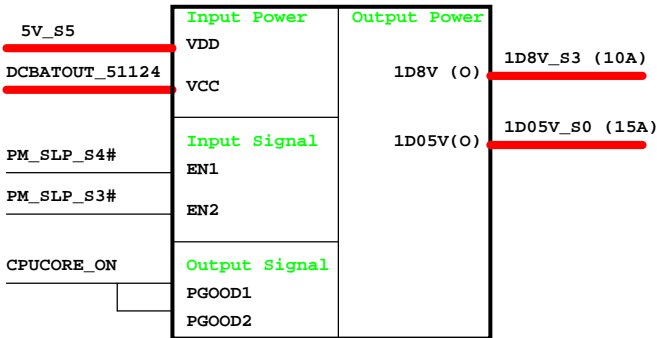


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緯創資通 Wistron Corporation 21F, 88, Sec 1, Hsin Tai Wu Rd., Hsinchu, Taipei Hsin 221, Taiwan, R.O.C.	
Title SATA & PATA ODD	
Size Custom	Document Number P08B1
Date: Friday, May 23, 2008	Sheet 29 of 50

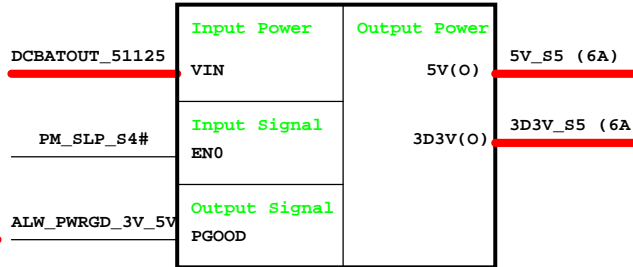
CPU_CORE
ISL6266A



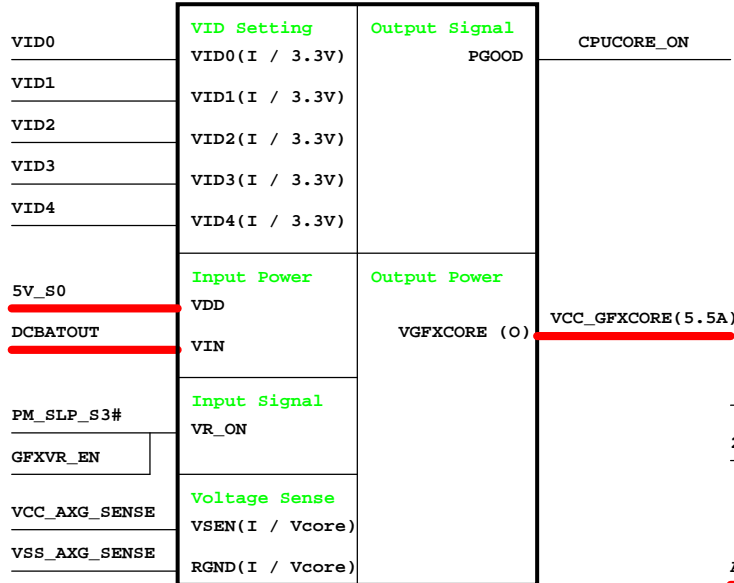
TPS51124
1D8V/1D05V



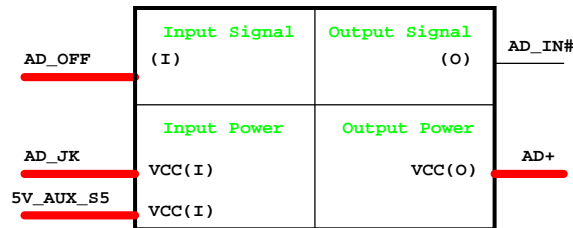
TPS51125
5V/3D3V



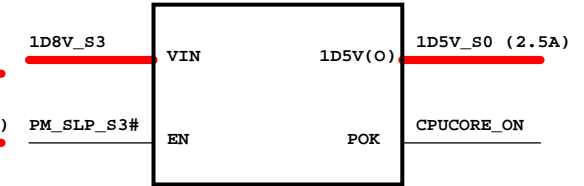
GFX_CORE
ISL6263A



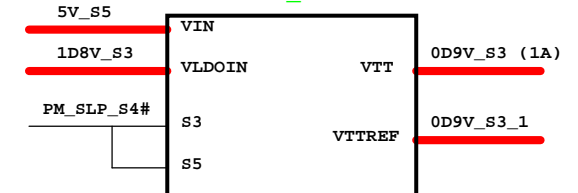
Adapter



APL5912
1D5V_S0



0D9V_S0



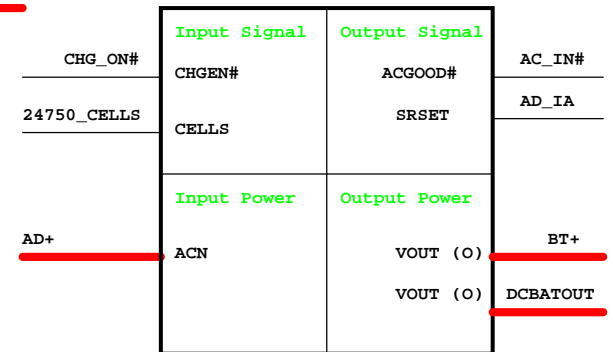
TPS51100

2D5V_S0



APL5913

Charger BQ24750



BOM

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Title

Power Sequence Logic

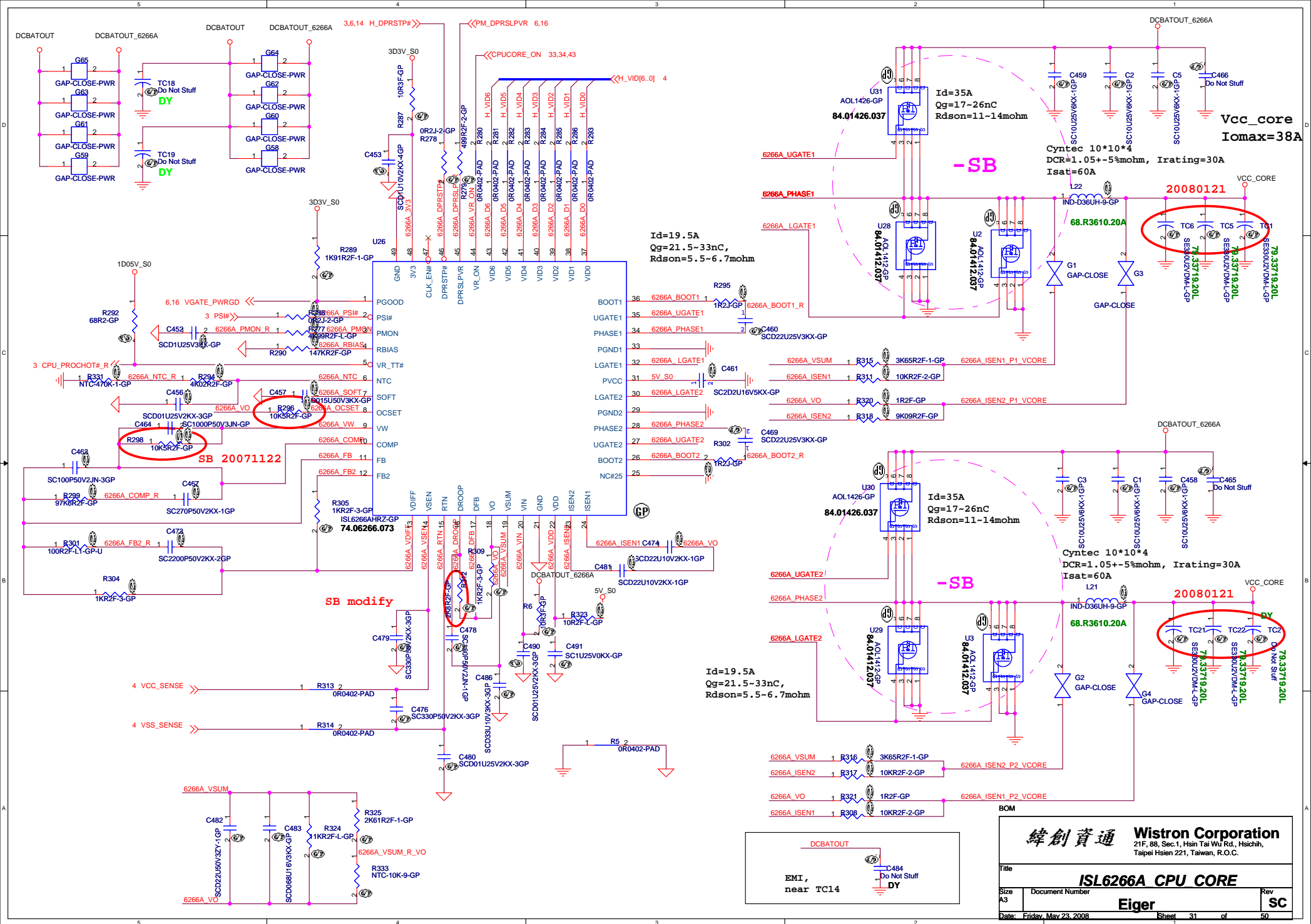
Size B Document Number

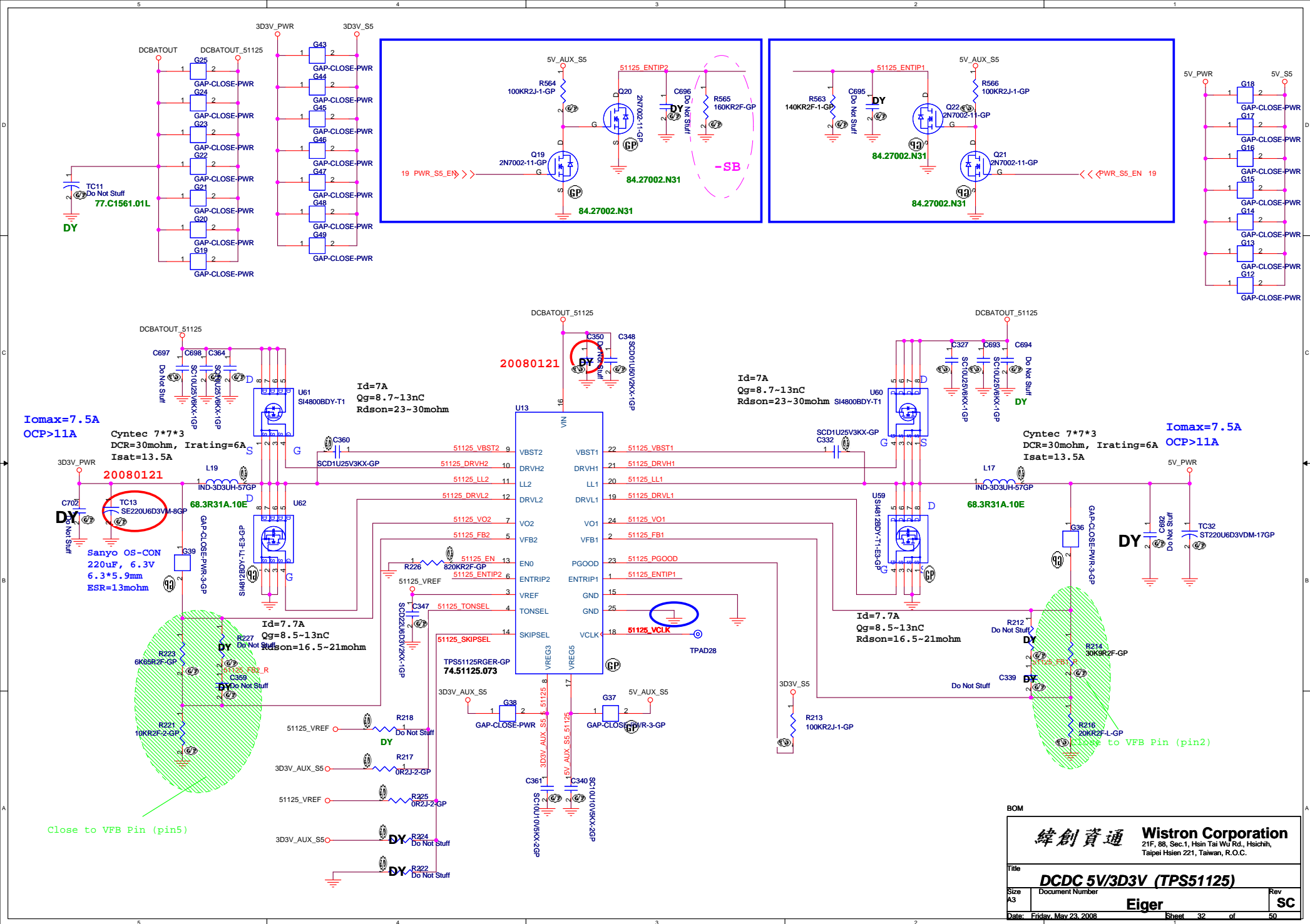
P08B1

Date: Friday, May 23, 2008

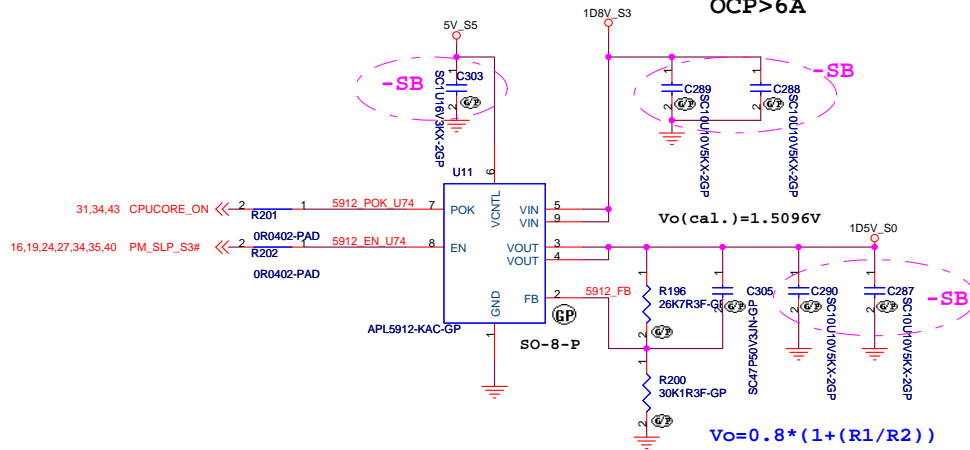
Sheet 30 of 50

Rev SA

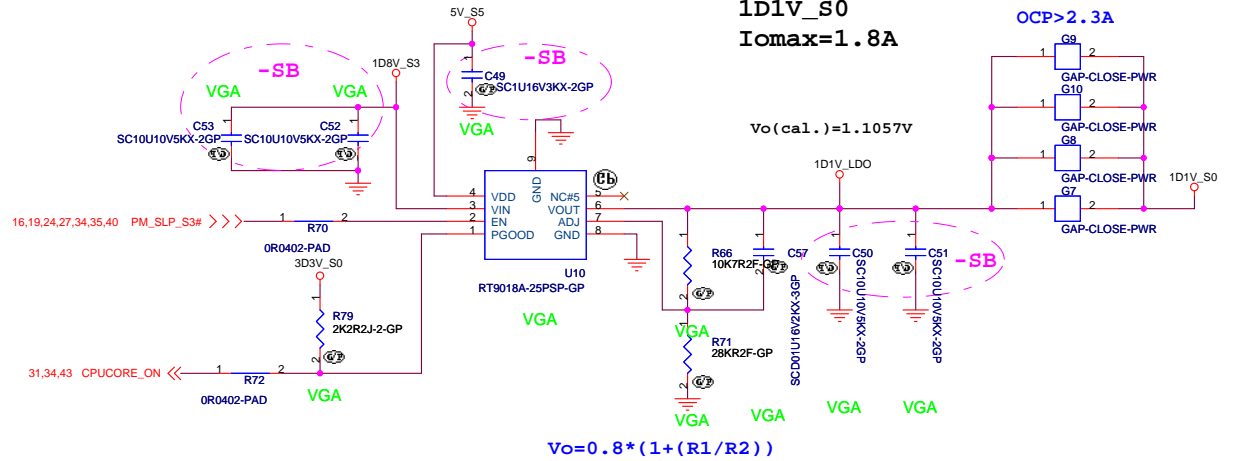




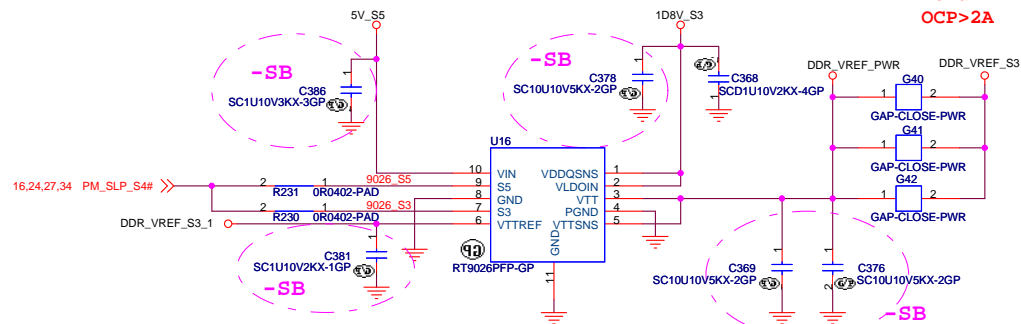
1D5V_S0
Iomax=3.5A
OCP>6A



1D1V_S0
Iomax=1.8A

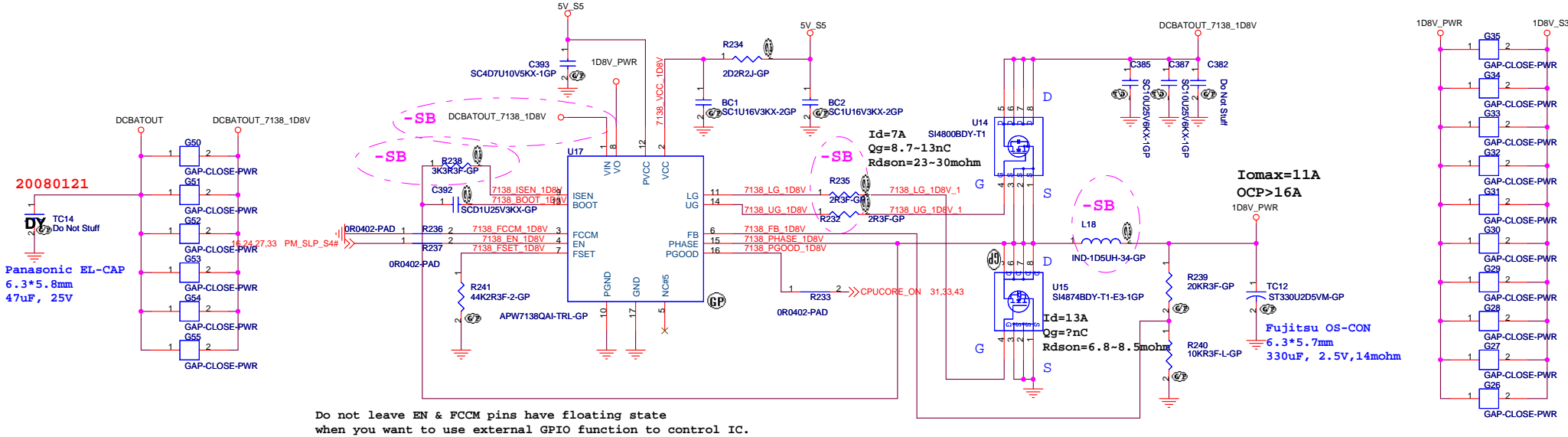


Iomax=1A
OCP>2A



BOM

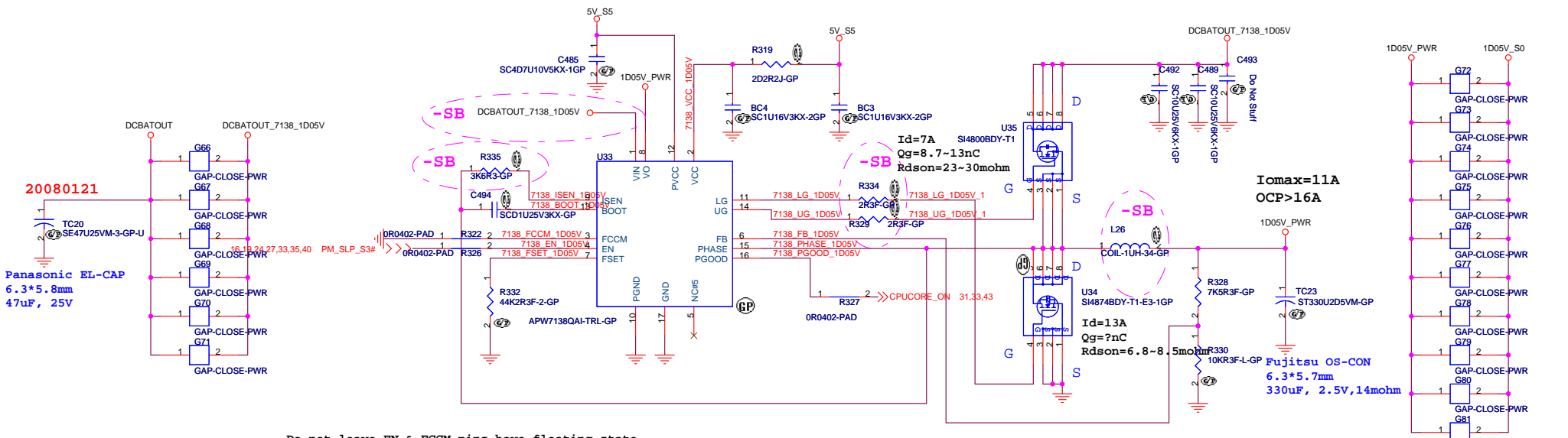
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
1D5V & 1D1V & 0D9V	
Size	Document Number
A3	P08B1
Date:	Rev
Friday, May 23, 2008	SA
Sheet	of
33	50



$$R_{fset} = 1 / (F_{sw} * K)$$

$$K = 75 * 10^{-12}$$

$$V_{out} = 0.6 * (1 + R_h / R_l)$$



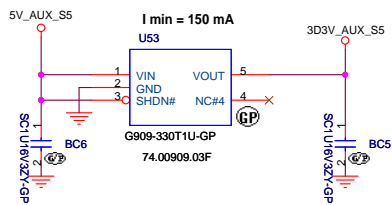
$$R_{fset} = 1 / (F_{sw} * K)$$

$$K = 75 * 10^{-12}$$

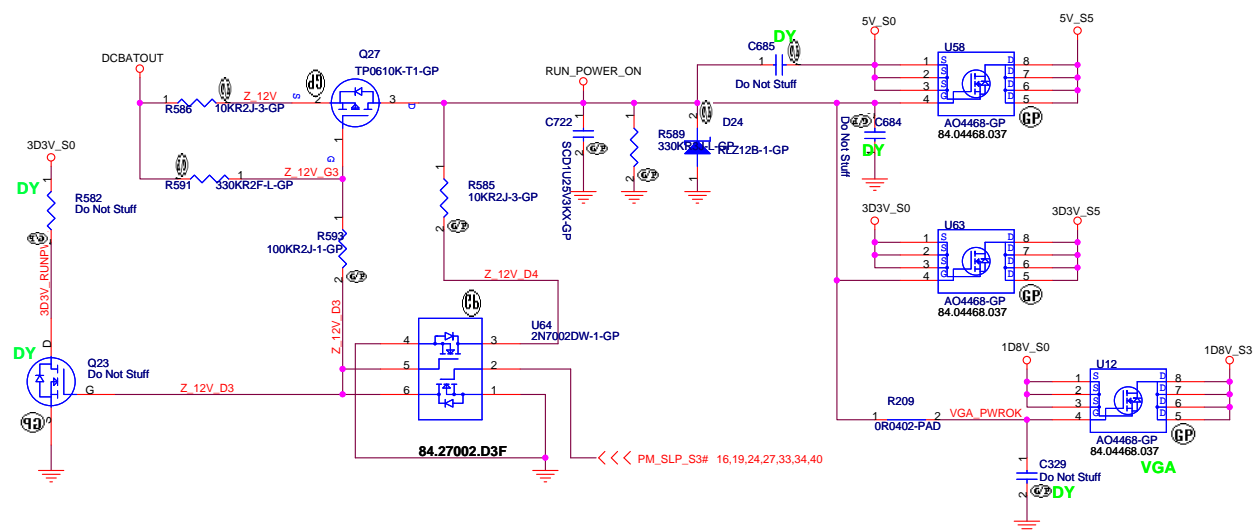
$$V_{out} = 0.6 * (1 + R_h / R_l)$$

BOM			
緯創資通 Wistron Corporation			
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Title			
APW7138 1D8V 1D05V			
Size	Document Number	Rev	
A3	P08B1	SA	
Date:	Friday, May 23, 2008	Sheet	34 of 50

Aux Power 3D3V_AUX_S5

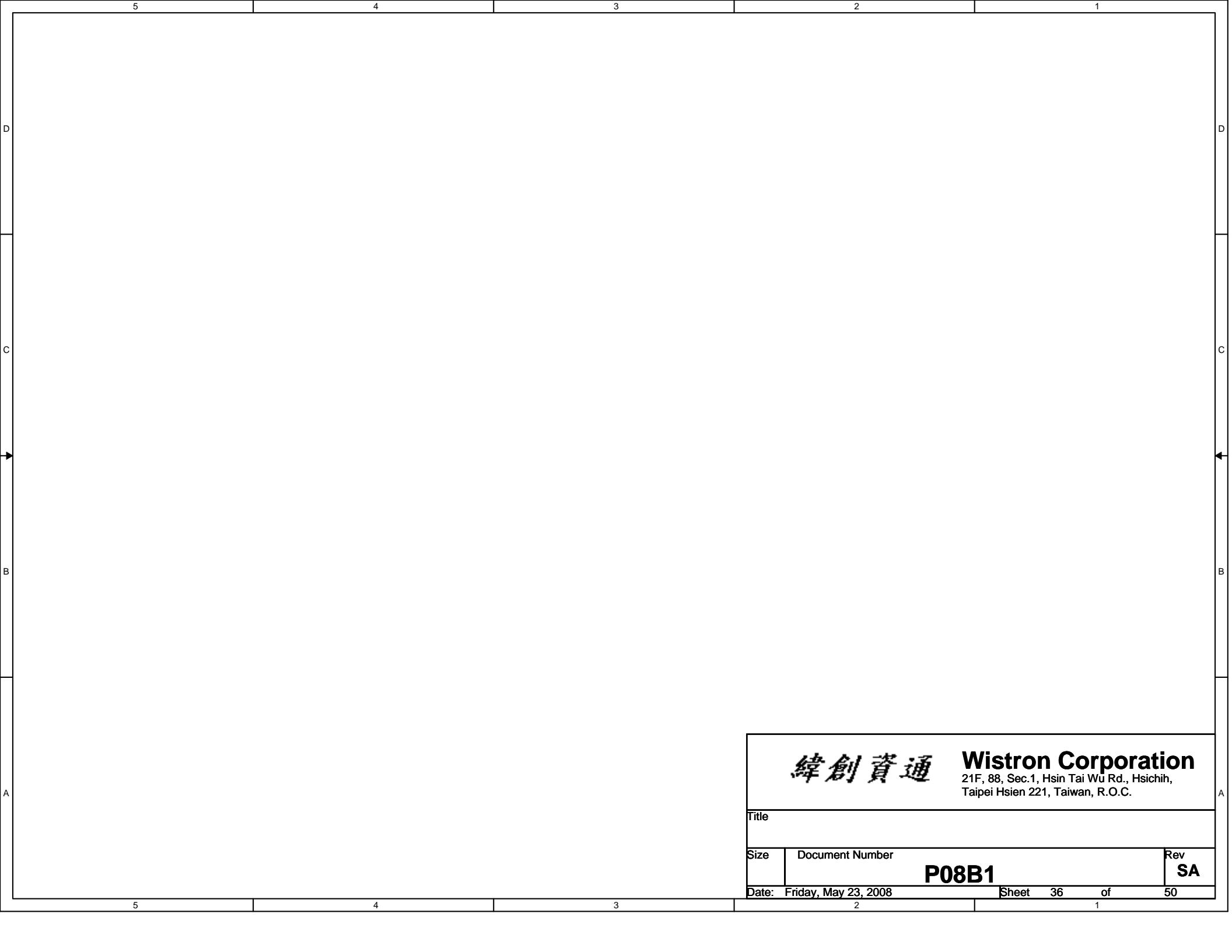


Run Power



BOM

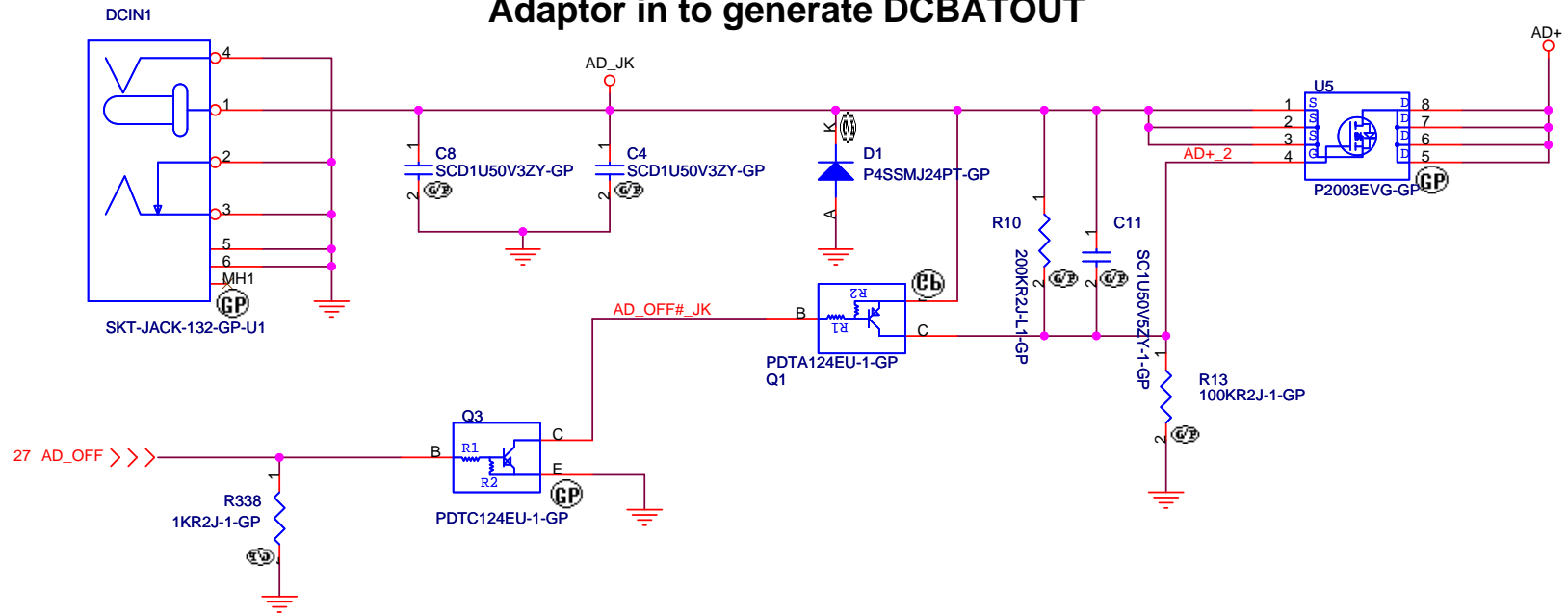
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Title RUN POWER and 3D3V_AUX_S5	
Size	Document Number
P08B1	
Date: Friday, May 23, 2008	Rev SA
Sheet 35	of 50



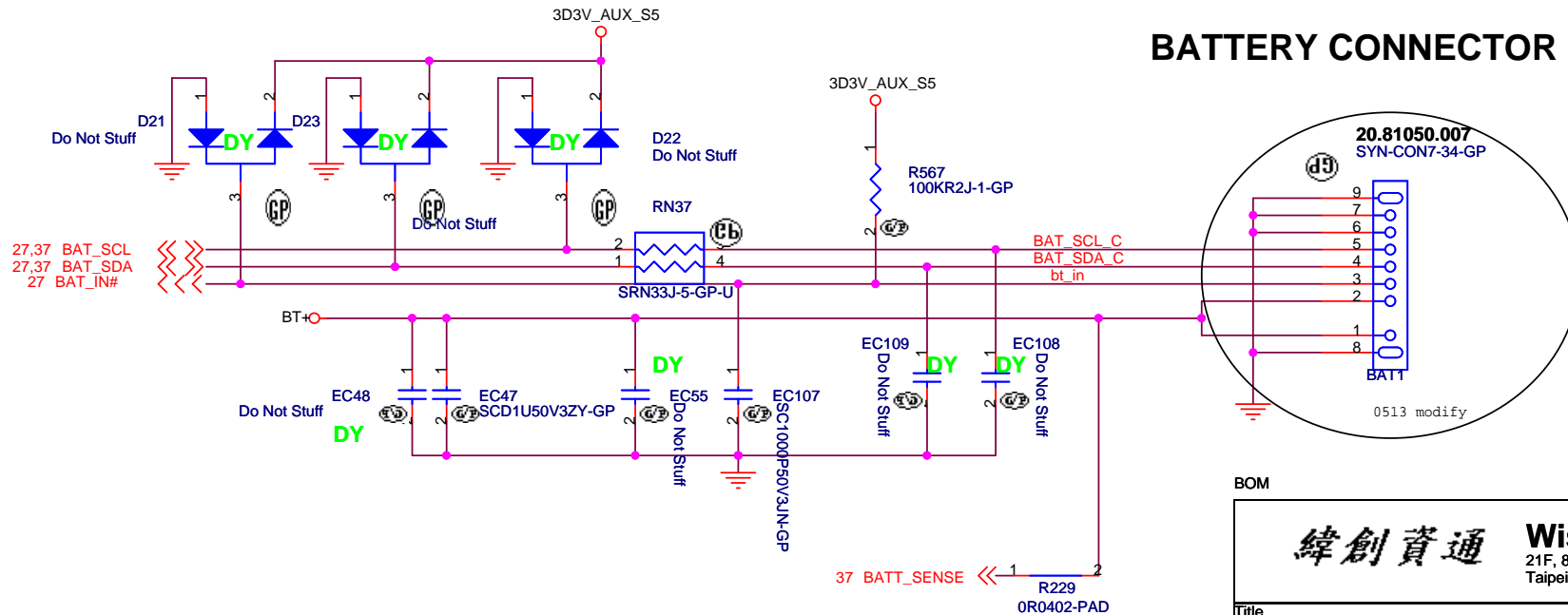
緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title		
Size	Document Number	Rev
	P08B1	SA
Date:	Friday, May 23, 2008	Sheet 36 of 50

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



BOM

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

AD/BATT CONN

Size

Document Number

P08B1

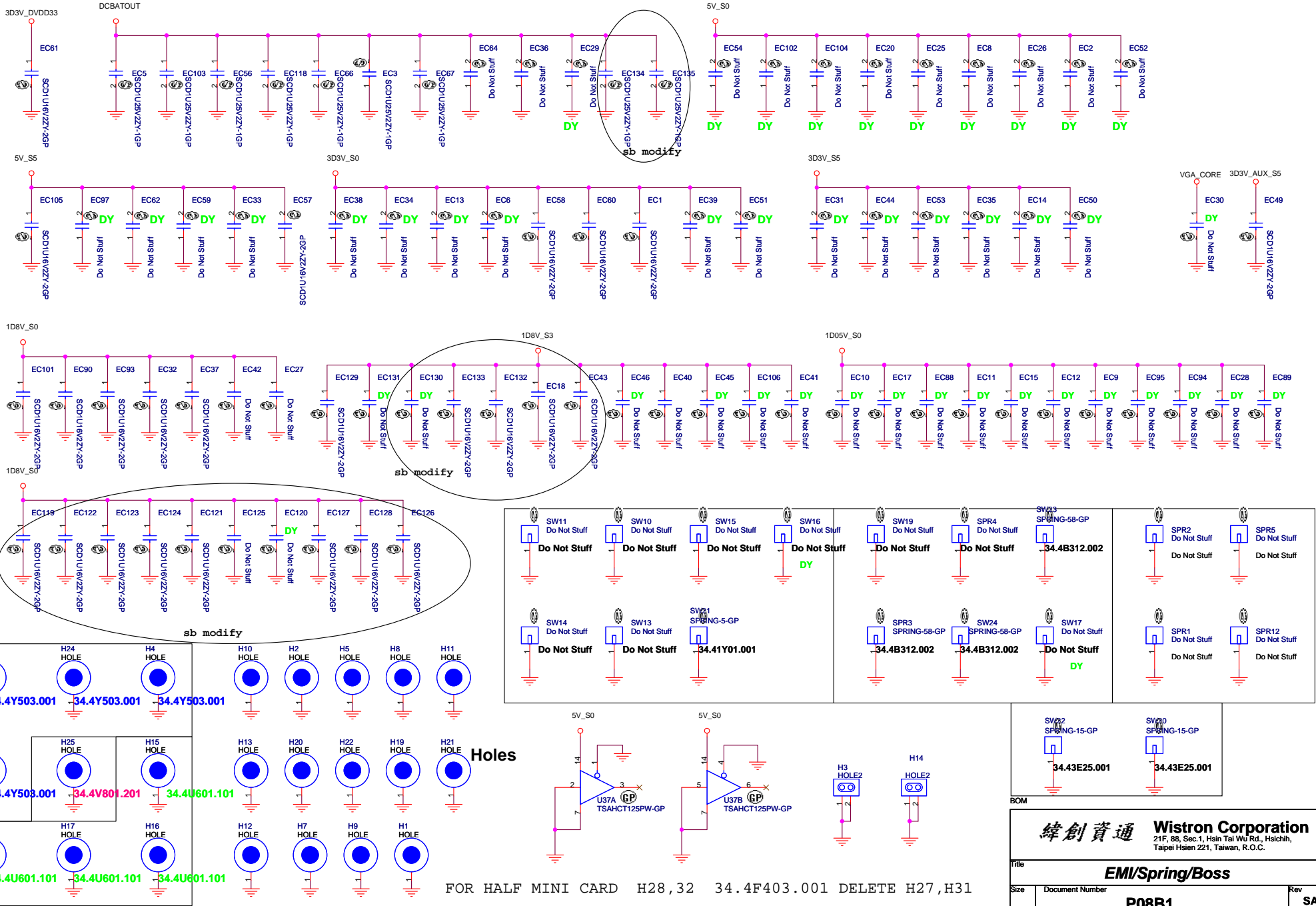
Rev

SA

Date: Friday, May 23, 2008

Sheet 38 of 50

EMI Caps

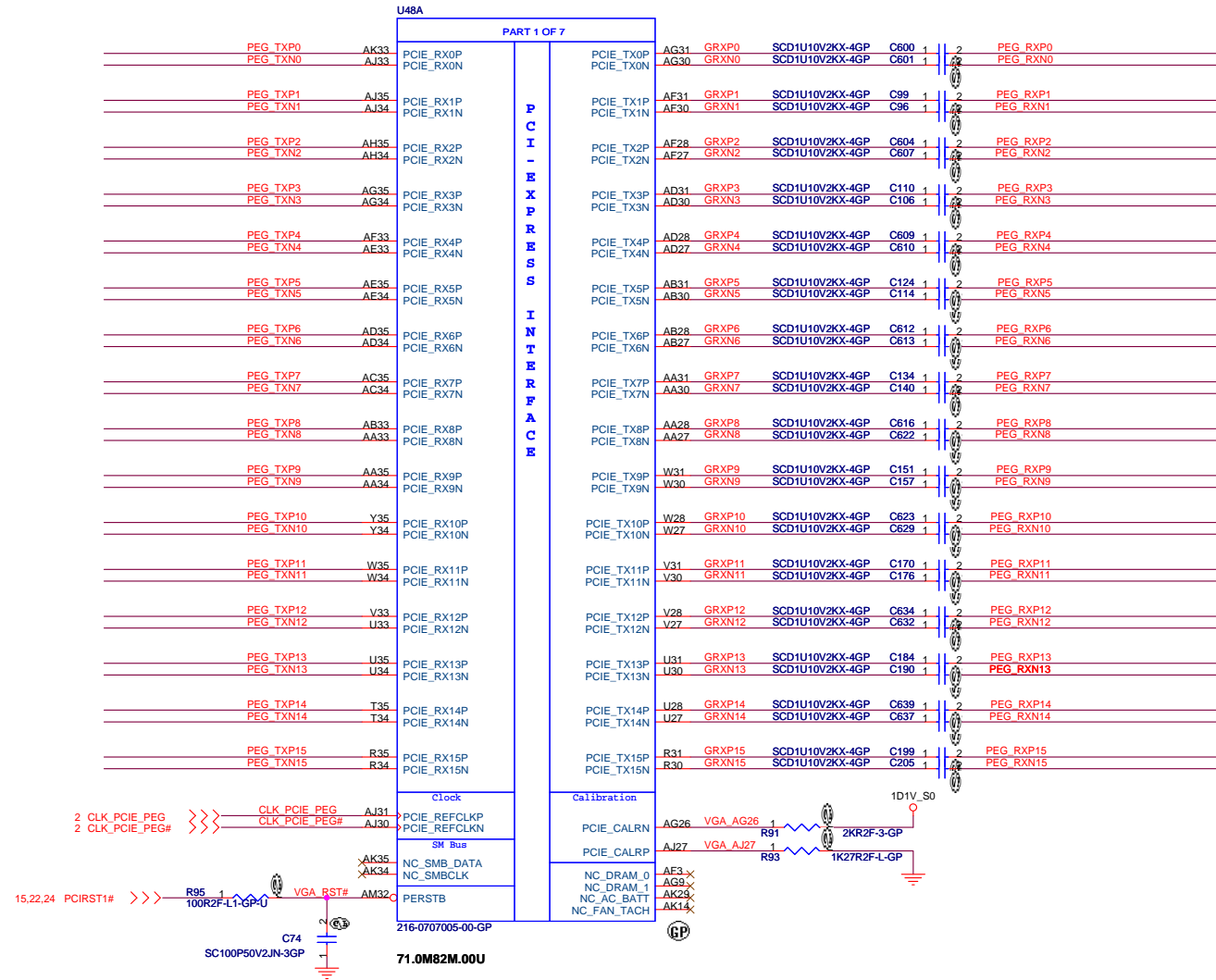


緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		EMI/Spring/Boss	
Size	Document Number	P08B1	Rev SA
Date: Friday, May 23, 2008	Sheet 39	of 50	

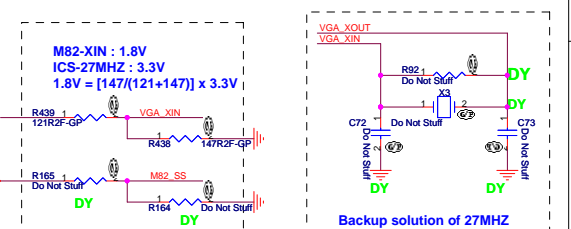
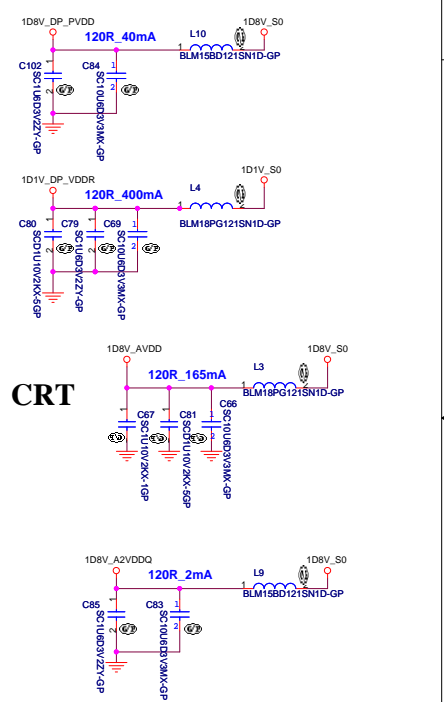
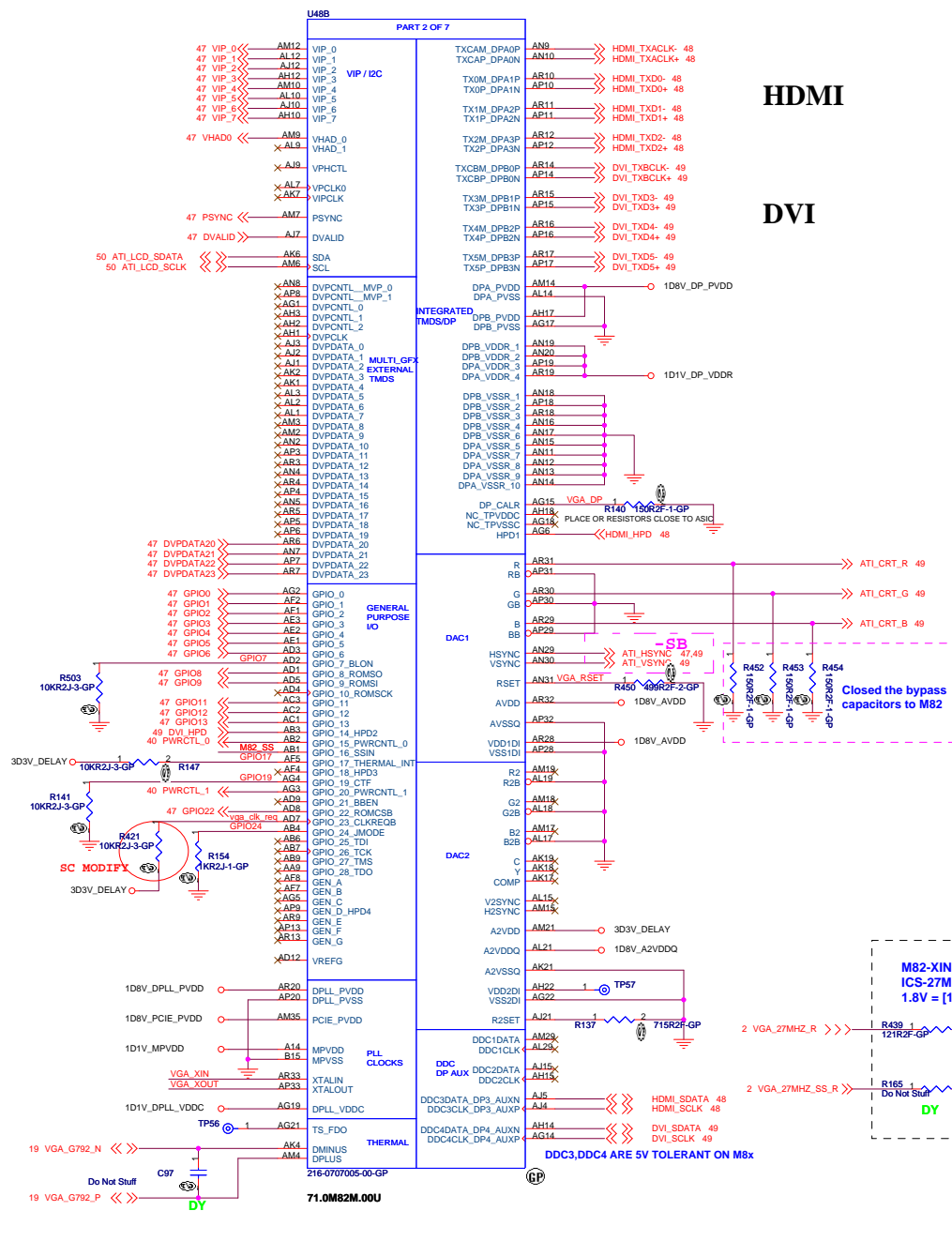
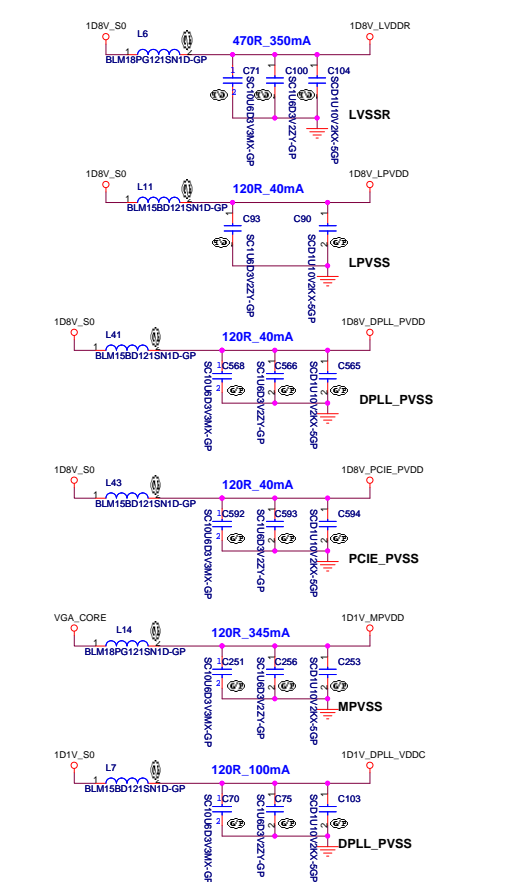
6 PEG_TXP[15..0] >>> PEG_TXP[15..0]
6 PEG_TXN[15..0] >>> PEG_TXN[15..0]

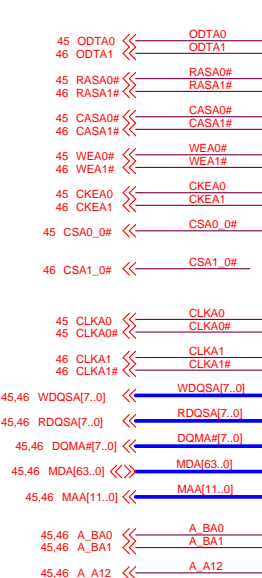
PEG_RXP[15..0] >>> PEG_RXP[15..0] 6
PEG_RXN[15..0] >>> PEG_RXN[15..0] 6



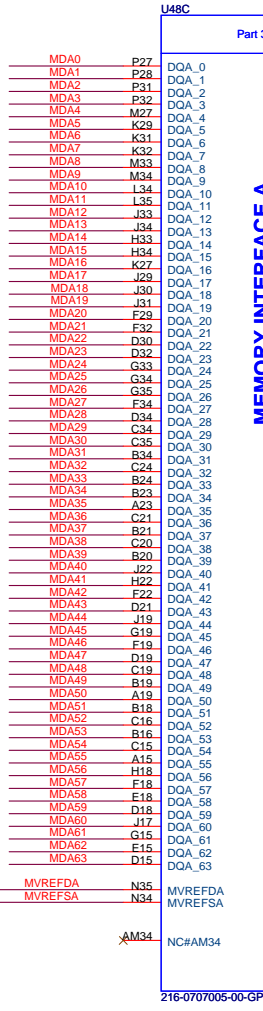
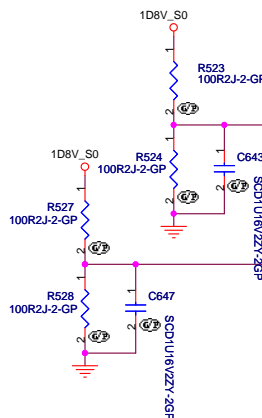
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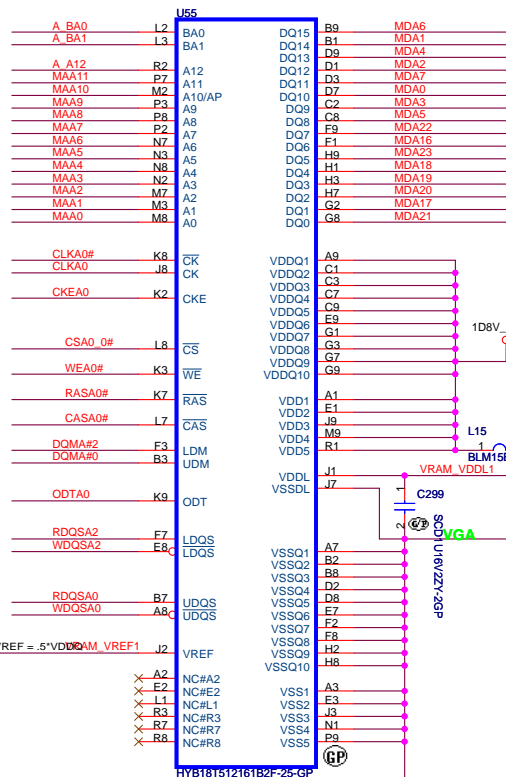
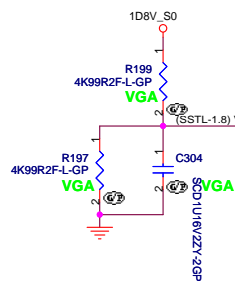
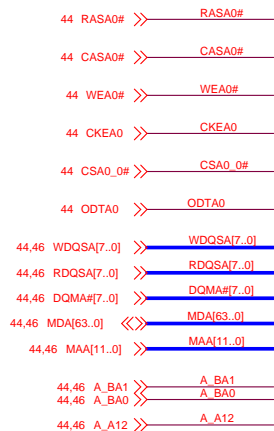
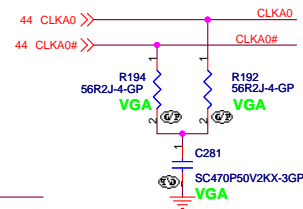
緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title		
M82MPE PCIEG(1)		
Size	Document Number	Rev
	P08B1	SA
Date: Friday, May 23, 2008		
Sheet 41 of 50		



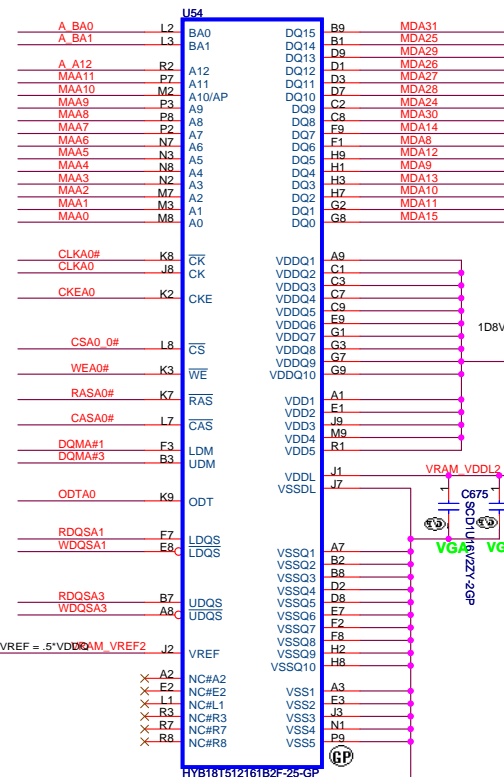


PLACE MVREF DIVIDERS AND CAPS CLOSE TO ASIC

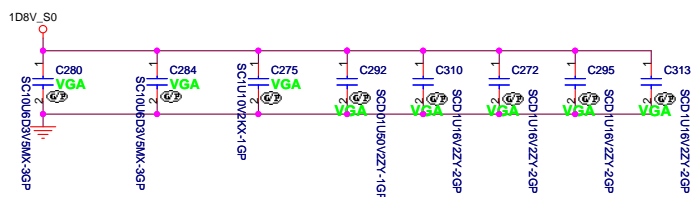
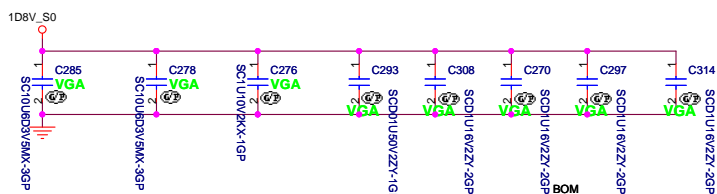




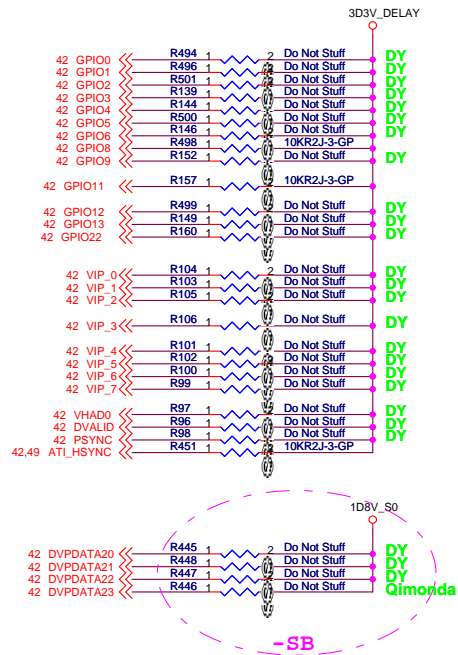
72.18512.M0U



72.18512.M0U



Note:1 VIP3 MUST NOT BE PULLED HIGH ON M82-M
Note:2 GPIO8 MUST NOT BE PULLED HIGH ON M86-M or M7X



CONFIGURATION STRAPS			RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1= INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE RSVD = ATI RESERVED (DO NOT INSTALL)	
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET				
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M8x	M7x
BIF_MSI_DIS	VIP1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_AUDIO_EN	VIP3	ENABLE HD AUDIO (M7XM and M86M ONLY) Note:1	X	X
BIF_64BAR_EN_A	VIP5	64 BIT BARS DISABLED	NA	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X	X
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO (M82M ONLY) Note:2	X	RSVD
BIF_GEN2_EN_A	GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X	0
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	NA	X
ROMIDCFG(3:0)	GPIO(13:11,9)	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XX X X	X X X X
VIP_DEVICE_STRAP_ENA	VSYN	IGNORE VIP DEVICE STRAPS	0	0
BIF_VGA_DIS	PSYN	VGA ENABLED	0	0
BIF_HDMI_EN	HSYN	HDMI ENABLE (SEE NOTE 2)	X	X
DEBUG_I2C_ENABLE	GPIO6	Internal use only	0	0
MEM_TYPE	ANY UNUSED GPIO OR DVP THAT ARE NOT CONFIG STRAPS FOR EXAMPLE DVPDATA20:23 IN THIS DESIGN	MEMORY TYPE,MAKE AND SIZE INFO	X X X X	X X X X

NOTE 1: HD AUDIO MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

NOTE 2: HDMI MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

VRAM ID TABLE

DVPDATA22 DVPDATA23	R447 R446	VRAM SELECTION
0 0	DY DY	HYNIX 72.55162.00U VRAM_H5P85162FFR(Rev03)
0 1	DY KEEP	Qimonda 72.18512.M0U VRAM_HYB18T512161B2F-25 TF
1 0	KEEP DY	Samsung 72.45116.A0U VRAM_K4N51163QE-2C25 FBGA84
1 1	KEEP KEEP	NA

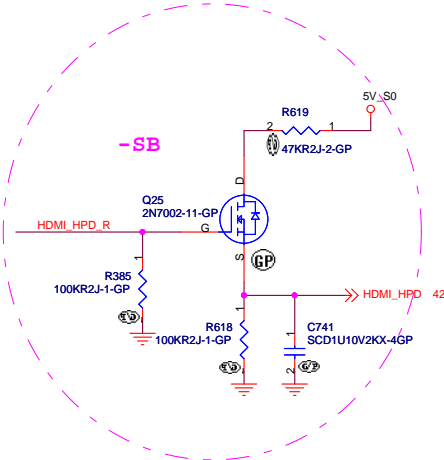
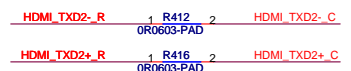
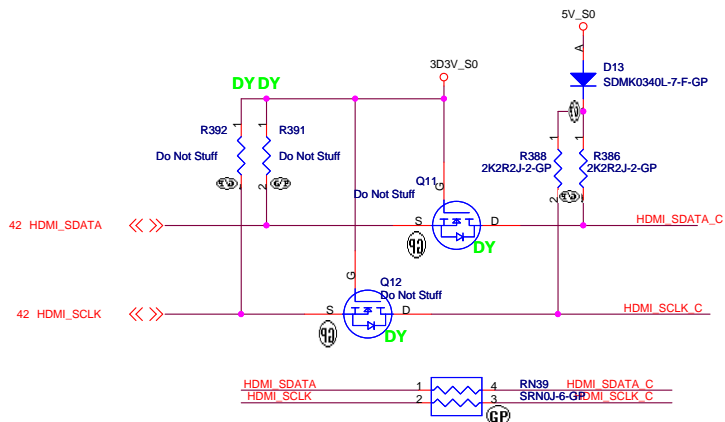
ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET

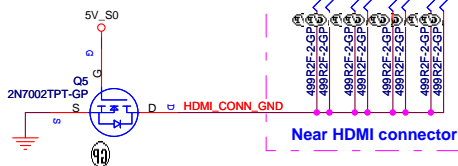
VHAD0	VIP0	VIP2	VIP4	VIP6	VIP7	GPIO2	GPIO3	H2SYNC
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOs ARE USED, THEY MUST NOT CONFLICT DURING RESET								
GPIO_28_TDO	GENERICC	GPIO21_BB_EN						

BOM

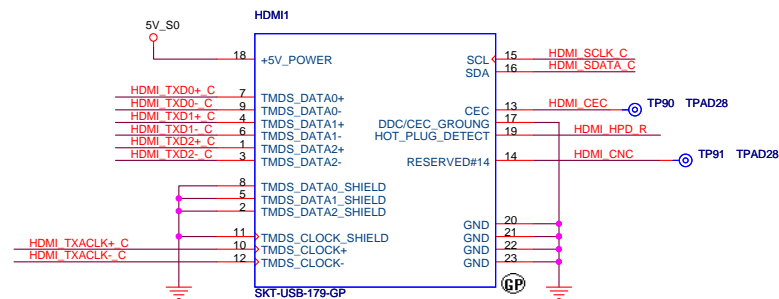
緯創資通 Wistron Corporation		
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title STRAPS		
Size A3	Document Number P08B1	Rev SA
Date: Monday, May 26, 2008	Sheet 47	of 50



MINIMIZE THE DISTANCE
BETWEEN THESE CAP to
M82.



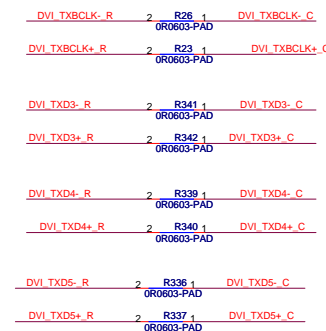
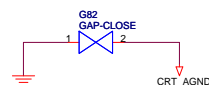
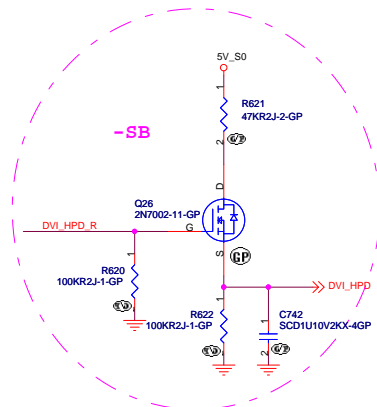
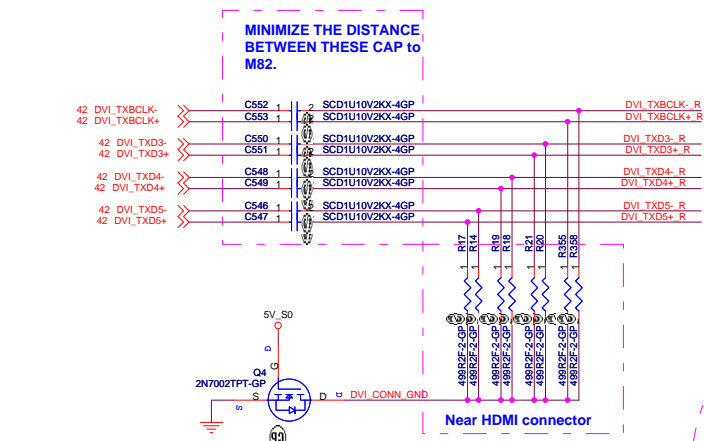
HDMI CONN



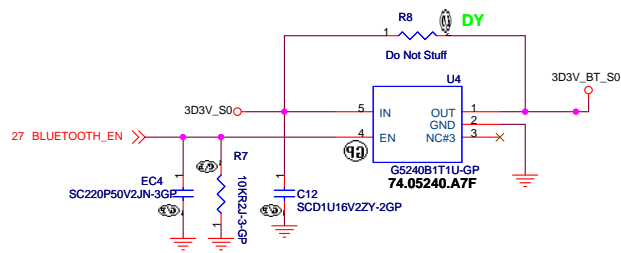
62.10078.121

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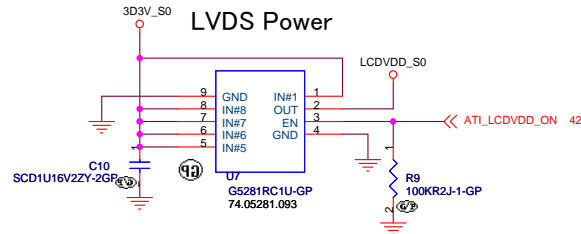
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
HDMI CONN	
Size	Document Number
A3	P08B1
Date:	Rev
Friday, May 23, 2008	SA
Sheet	of
48	50



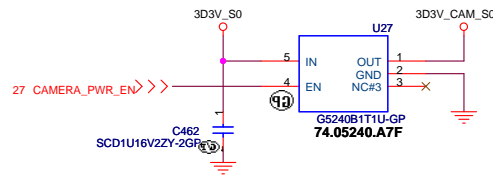
Blue Tooth Power



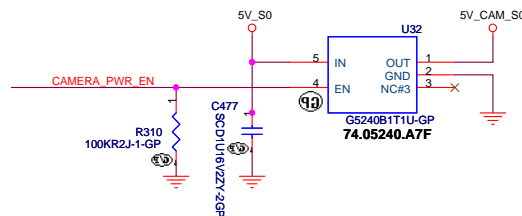
LVDS Power



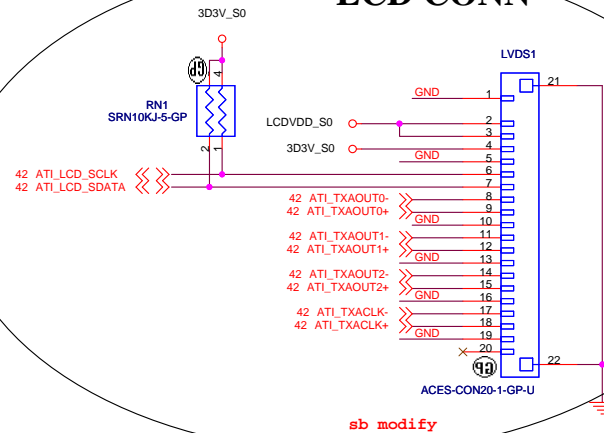
WEBCAM Power for LITE-ON



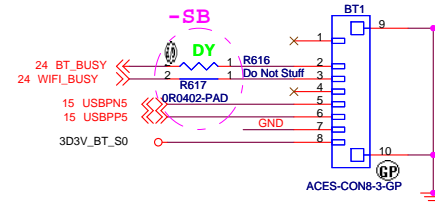
WEBCAM Power for Chicony



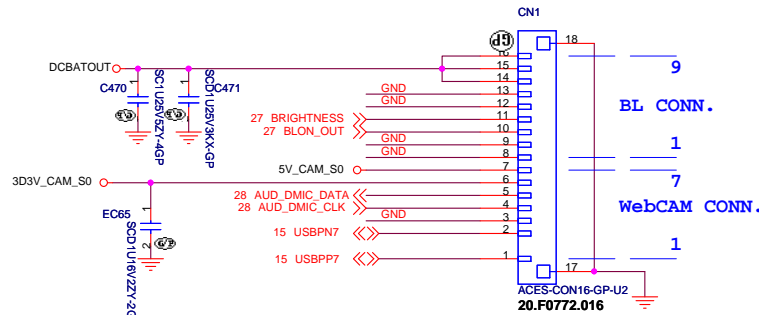
LCD CONN



BT CONN



WEB & BL



BOM

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Title	WEBCAM & LCD CONN
Size A3	Document Number
	P08B1
Date: Friday, May 23, 2008	Rev SA
Sheet 50 of 50	